2016 International Workshop for Ultra Low Power Nano-electronics for IoT

October 18-19, 2016
International Conference room, 6th Floor, HIT Bldg.,
Hanyang University, Seoul, Korea

Ultra low power nano-electronics is a vital element for IoT. This topic is chosen as the title of workshop because USA and EU have started unique R&D programs to develop the ultra low power nano-electronics and Korea also has the same strategic plan to achieve ultra high performance and ultra low power at the same time. Under the same plan, this workshop will be an international forum to discuss and exchange ideas about low power nano-electronics with world class experts. 11 distinguished speakers are invited from EU, USA, Japan, and Korea. Absolutely, this workshop will be a good opportunity to open the possibility of future technology in the IoT fields and benefits for PhD students and field engineers since it is also linked with Nano KISS designed as lecture courses of advanced nano-electronics.

Hosted by

한양대학교 HANYANG UNIVERSITY

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KINN 국가나노인프라협의체 Korea Infrastructure Organization for Nanotechnology

NANO KISS KOREAN INTERNATIONAL SUMMER SCHOOL ON NANOELECTRONICS

Supported by

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2016 초저전력 반도체 기술 워크샵

2016년 10월 18-19일
한양대학교 종합기술원 (HIT) 6층 국제회의장

인공지능과 사물인터넷 시대에 필요한 정보기기와 부품의 급증추세는 그 전력소모가 조만간 감당하기 어려운 수준에 이를 것이라는 예상이 있으나, 우리나라에서는 아무도 이야기하지 않는 이러한 에너지 문제에 대한 근본적인 대책이 절실히 필요한 상황입니다.

미국과 유럽에서는 초저전력 반도체 기술에 대한 중요성을 인식하고 연구개발 투자를 하고 있는데 비해, 우리나라에서는 투자우선 순위에서 외면을 받고 있는 상황입니다. 이에 세계 각국의 해당분야 석학 11명을 초청하여 초저전력 반도체소자 기술에 대한 연구개발 현황을 파악하고, 앞으로 우리나라의 연구개발 투자방향에 참고하기 위해 본 워크샵을 기획하였습니다.

정부 관계자, 산/학/연의 전문가, 그리고 미래 우리나라의 주역이 될 학생들까지 함께 모여 우리나라의 미래를 이끌어 갈 중요한 논의에 참여해 주시기를 바랍니다.

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Scientific Program - Day 1

Tuesday, 18 October 2016 Memory devices, analog design and technologies	
09:00-09:30	Registration
09:30-10:00	Opening Remarks
	(Session Chair: TBD)
10:00-11:15	**Capacitor-less memory: advances and challenges** Prof. Francesco Gamiz *(Univ. of Granada, Spain)*
11:15-11:30	Break
11:30-12:45	**Technology options for high energy efficiency with FDSOI** Dr. Fred Allibert *(SOITEC, France)*
12:45-14:00	Lunch
	(Session Chair: TBD)
14:00-15:15	**Low-power analog design fundamentals** Prof. Bram Nauta *(Univ. of Twente, Netherlands)*
15:15-15:30	Break
15:30-16:30	**Steep-slope transistor concepts for low-power CMOS** Prof. Jurriaan Schmitz *(Univ. of Twente, Netherlands)*
16:30-17:00	**Sharp switching devices based on band modulation** Prof. Sorin Cristoloveanu *(Grenoble INP Minatec, France)*
17:00-17:15	Break
17:15-18:30	**Technology Challenges and Opportunities of Mobile Memory** Dr. Seok-Hee Lee *(SK Hynix, Korea)*
18:30-20:30	Banquet

Scientific Program - Day 2

Wednesday, 19 October 2016 Off the beaten CMOS path	
08:30-09:30	Registration
	(Session Chair: TBD)
09:30-10:45	**Non-Si MOSFET and TFET for low-power circuits** Prof. Shinichi Takagi *(Univ. of Tokyo, Japan)*
10:45-11:00	Break
11:00-12:15	**Synaptic devices and neuron circuits for neuromorphic chips** Prof. Byung-Gook Park *(Seoul National Univ., Korea)*
12:15-13:30	Lunch
	(Session Chair: TBD)
13:30-14:45	**Taking Gallium Nitride HEMTs into the THz** Prof. Debdeep Jena *(Cornell Univ., USA)*
14:45-15:00	Break
15:00-16:15	**Charge Trapping and Time-dependent Variability in Low-Voltage MOS Transistors** Prof. Tibor Grasser *(Technical Univ. of Vienna, Austria)*
16:15-16:30	Break
16:30-17:45	**Photonics on CMOS is Key Enabling Technology for innovation** Dr. Maryse Fournier *(LETI, France)*
17:45-18:15	Wrap up & Closing remark

Registration

1. 등록방법

등록신청서를 작성하신 후 한양대학교로 회신하여 주십시오.
(E-mail: solewolp@hanyang.ac.kr 또는 Fax 02-2220-2503)

등록신청서는 한양대학교 산학협력단 홈페이지에서 받으실 수 있습니다.
(http://research.hanyang.ac.kr)

2. 등록비

10월 10일(월)까지 등록비를 입금하여 주십시오.

- 일반: 300,000원
- 학생: 150,000원

※ 학생등록자는 등록신청서 회신 시 학생임을 증명하는 자료(재학증명서, 학생증 사본 등)를 제출해 주십시오.

3. 결제방법

<사전등록>

송금

계좌번호: 100-030-692992
은 행: 신한은행
통 장 명: 한양대학교 산학협력단

<현장등록>

카드결제 및 송금

※ 취소/환불규정: 등록취소는 이메일(solewolp@hanyang.ac.kr)을 통해 반드시 서류상으로 요청하셔야 합니다.
등록비 환불은 대회 종료 후 집행됩니다.

Venue & Travel

How to get to Hanyang

2 Subway Line 2, Hanyang Univ. station, Exit #2

B Blue Bus: 302, 410

G Green Bus: 2012(cheongryangri), 2013, 2014, 2222

Address

[133-791] 서울특별시 성동구 왕십리로 222
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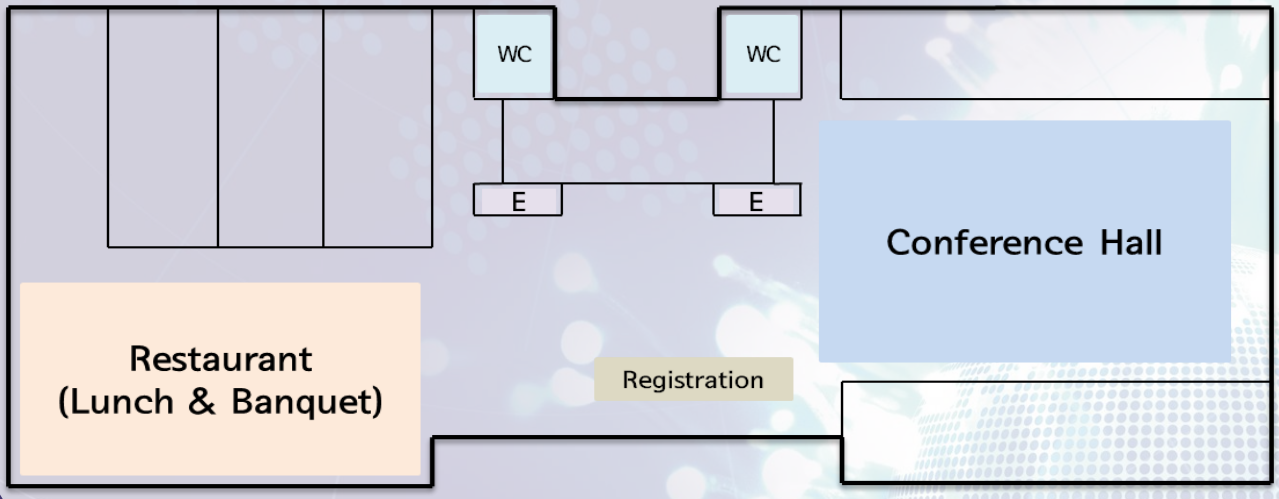
222 Wangsimni-ro, Seongdong-gu, Seoul, 04763, Korea
Hanyang Institute of Technology (HIT), Hanyang University

Venue & Travel

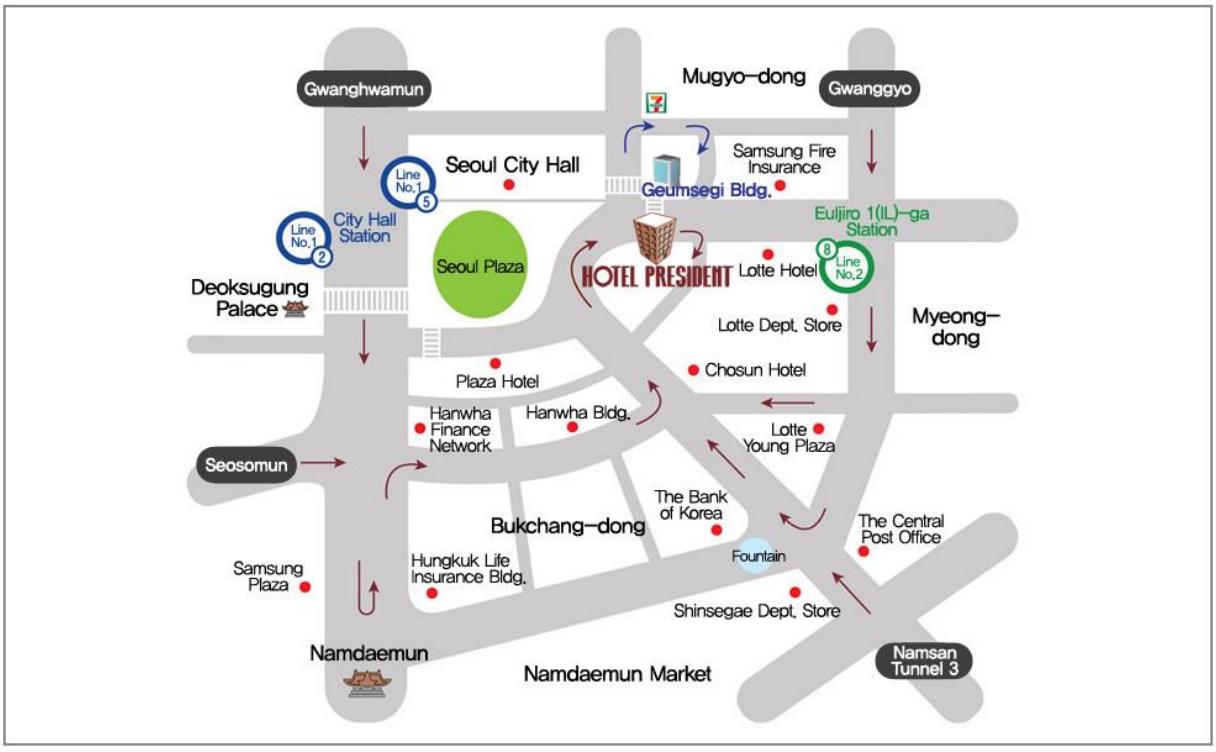
Map: HIT(Hanyang Institute of Technology) Building

Map: 6th Floor of HIT(Hanyang Institute of Technology) Building



Venue & Travel

Welcome to Hotel President



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TELEPHONE : +82-2-753-3131

From Incheon International Airport (As of June 1, 2014)	
KAL Limousine Bus (No. 6701)	- Incheon International Airport → Koreana Hotel → Plaza Hotel → Lotte Hotel (Hotel President) - Time : Approximately 1 hour 20 minutes (2-minute walking distance to Hotel President) - Fare : Adult KRW 16,000, Children (6~12 years old) KRW 10,000 - Get on the bus at East side 4B, West side 11A station
Subway	- Incheon International Airport (Airport Railroad) → Hongik University Entrance (Transfer to Line No. 2) → Eulgiro 1(IL)-ga Entrance (Exit No. 8) - Time : Approximately 1 hour and 9 minutes - Fare : Card KRW 4,150, Cash KRW 4,250

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Chair persons

Jinho Ahn(Hanyang Univ.)
Yong Tae Kim(KIST)
Jo-Won Lee (Hanyang Univ.)
Sorin Cristoloveanu(INPG, France)

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Eun-Soo Nam (ETRI)
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Acknowledgements

This workshop is partly supported by the National research foundation of Korea grant funded by the Korea government (NRF-2016K1A3A1A21005751)

Invited Speakers

1.	Prof. Francesco Gamiz *(Univ. of Granada, Spain)*
2.	Dr. Fred Allibert *(SOITEC, France)*
3.	Prof. Bram Nauta *(Univ. of Twente, Netherlands)*
4.	Prof. Jurriaan Schmitz *(Univ. of Twente, Netherlands)*
5.	Prof. Sorin Cristoloveanu *(INPG, France)*
6.	Dr. Seok-Hee Lee *(SK Hynix, Korea)*
7.	Prof. Shinichi Takagi *(Univ. of Tokyo, Japan)*
8.	Prof. Byung-Gook Park *(Seoul National Univ., Korea)*
9.	Prof. Debdeep Jena *(Cornell Univ., USA)*
10.	Prof. Tibor Grasser *(Technical Univ. of Vienna, Austria)*
11.	Dr. Maryse Fournier *(LETI, France)*

Invited Speakers

Prof. Francesco Gamiz
(Univ. of Granada, Spain)

Francisco Gamiz received his B.S. degree in PHYSICS in 1991, and his Ph.D. degree in 1994 from the University of Granada, both with Honors (Best Student Award). Since 1991 he has been working on the study of the transport properties in semiconductor heterostructures. His current research interests include the study of silicon-on-insulator devices, quantum transport and memory effects, graphene and pseudoMOS based sensors, and TMDs and van der Waals heterostructures. In 1999 he was Visiting Researcher at the IBM T.J. Watson Research Center (USA). He has also has developed several research visits at MINATEC in Grenoble (France) and TU-Wien (Austria). Since 2005, he is Full Professor of Electronics, and since 2008, Head of Nanoelectronics and Graphene Research Labs at UGR. He was co-ordinator of FP6-EUROSOI and FP7-EUROSOI+ projects, and has participated in FP6-SINANO and FP7-NANOSIL Networks of Excellence, and in REACHING-22 project, awarded with Catrene Label, and leaded by STMicroelectronics and CEA-LETI. In H2020, Prof. Gamiz is coordinator of REMINDER European project, and participates in ECSEL-WAYTOGO-FAST project and in EU-NEREID. Prof. Gamiz is member of the User Committee of H2020-EU-ASCENT Project.

He has adviced 15 PhD dissertations, and has co-authored more than 300 refereed papers in major journal and international conference proceedings, several book chapters, and he is co-holder of several international patents related to multi-body 1T-DRAM. His publications have received more than 3600 cites (h-index=32, Google scholar). Prof. Gamiz has given more than 20 invited conferences about nanoelectronics, including Massachusetts Institute of Technology (MIT), and Tokyo Institute of Technology (TiTech) and MINATEC-Grenoble. Prof.Gamiz is Senior Member of the Electron Device Society of the IEEE. He is member of different Steering/Technical Committees of International Conferences such as European Solid State Device Research Conference, European Siliconon- Insulator Technology Workshop, SOI Symposium of the Electrochemical Society (USA) and VLSI-TSA Conference in Taiwan. He has received several Prizes and Awards.

Abstract

Capacitor-less memory: advances and challenges

Several types of floating-body capacitorless 1T-DRAM memory cells with planar SOI or multi-gate 3D configurations are reviewed and compared. We focus on the recently proposed concepts (MSDRAM, A2RAM and Z^2-FET), by addressing the device architecture and fabrication, operating mechanisms, and scaling issues. Experimental results together with numerical simulations indicate the directions for performance optimization, and their implementation in FDSOI 28nm (FD28) and FDSOI 14nm (FD14) technological nodes. These memory cells are the basis for the recently started European Project REMINDER "Revolutionary Embedded Memory for INternet of Things Devices and Energy Reduction". REMINDER aims to develop an embedded DRAM solution optimized for ultra-low-power consumption and variability immunity, specifically focused on Internet of Things (IoT) cut-edge devices. REMINDER is based on three pillars:

Investigation (concept, design, characterization, simulation, modelling), selection and optimization of a Floating-Body memory bit cell in terms of low power and low voltage, high reliability, robustness (variability), speed, reduced footprint and cost. Fabrication of selected bit cells with FDSOI and III-V technologies.

i) Design and fabrication in FD28 and FD14 technology nodes of a memory matrix based on the optimized bit-cells developed in the first pillar. Matrix memory subcircuits, blocks and architectures will be carefully analysed from the power-consumption point of view. In addition variability tolerant design techniques underpinned by variability analysis and statistical simulation technology will be considered.

ii) Demonstration of a system on chip (SoC) application using the developed memory solution and benchmarking with alternative embedded memory blocks.

The eventual replacement of Si by strained Si/SiGe and III-V materials in future CMOS circuits would also require the redesign of different applications, including memory cells, and therefore we also propose the evaluation of the optimized bit cells developed in pillar i) in FD28 and FD14 technology nodes using these alternative materials. In order to achieve these goals, we adopt a multiscale approach that enables us to determine the band structures and the memory mechanisms (Band-to-Band Tunnelling, carrier transport and generation-recombination) in semiconductor NWs with different materials and geometries (Si, sSi, Si/Si-Ge core-shell, and III-V). We will employ numerical tools at different levels from atomic-detail (DFT) to the effective mass approximation.

We will sumarize the state-of-the-art, the objectives, challenges, risks, and the proposed tasks to fullfill the goal of REMINDER Project.1

Invited Speakers

Dr. Fred Allibert
(SOITEC, France)

Dr. Fred Allibert received his MS degree from the National Institute for Applied Sciences (INSA, Lyon, France) in 1997 and his PhD from Grenoble Polytechnic's Institute (INPG) in 2003, focusing on the electrical characterization of Unibond wafers and the study of advanced device architectures, such as planar double-gate and 4-gate transistors.

He was a visiting scientist at KAIST (Taejon, Korea) in 1998 and joined Soitec in 1999. As an R&D scientist, he implemented SOI-specific electrical measurement techniques (for thin films, multi-layers, high-resistivity) and supported the development of products and technologies targeting various applications, including FDSOI, RF, imagers, and high-mobility materials.

As Soitec's assignee at the Albany Nanotech Center (NY, USA), from 2011 to 2015, his focus was on substrate technologies for advanced nodes, exploring the benefits of different substrate materials and configurations for various device architectures.

In July 2015, he joined Soitec's Advanced R&D group as a senior scientist. He currently supports material and substrate development by exploring the substrate-device interactions, in various fields of micro-electronics, including RF and logic.

Abstract

Technology options for high energy efficiency with FDSOI

We live in a world where everyone and everything is connected through devices that range from the standalone outdoors sensor which sends simple information a few times a day to datacenters which store and compute massive amounts of information.

They share a common concern related to power consumption, be it to save battery life or reduce the utility bill, but have very different requirements in terms of performance and power management.

In this tutorial we will present different ways to reduce the power consumption at the device level using the FDSOI technology.

FDSOI devices benefit from key advantages which are (i) Excellent electrostatic control, (ii) reduced VT variability, (iii) good compatibility with high mobility materials and (iv) dynamically tunable VT. These, in turn, enable specific process optimization and centering as well as power management schemes.

We will also review the relevant SOI material properties such as layer thickness uniformity and BOX electrical properties.

Invited Speakers

Prof. Bram Nauta
(Univ. of Twente, Netherlands)

Bram Nauta was born in 1964 in Hengelo, The Netherlands. In 1987 he received the M.Sc degree (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven the Netherlands. In 1998 he returned to the University of Twente, where he is currently a distinguished professor, heading the IC Design group. His current research interest is high-speed analog CMOS circuits, software defined radio, cognitive radio and beamforming.

He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC), and was the 2013 program chair of the International Solid State Circuits Conference (ISSCC). He is currently the Vice president of the IEEE Solid-State Circuits Society.

Also, he served as Associate Editor of IEEE Transactions on Circuits and Systems II (1997-1999), and of JSSC (2001-2006). He was in the Technical Program Committee of the Symposium on VLSI circuits (2009-2013) and is in the steering committee and programme committee of the European Solid State Circuit Conference (ESSCIRC). He served as distinguished lecturer of the IEEE and is fellow of IEEE. He is co-recipient of the ISSCC 2002 and 2009 "Van Vessem Outstanding Paper Award" and in 2014 he received the 'Simon Stevin Meester' award (500.000€), the largest Dutch national prize for achievements in technical sciences.

Abstract

Low Power Analog Design Fundamentals

In this tutorial the fundaments of power dissipation and noise scaling of analog circuits will be discussed. It will be shown that for a given signal-to-noise ration and a certain bandwidth there are fundamental limits to power dissipation. A practical impedance scaling method that basically works for any analog circuit will be illustrated. This scaling method will give a deeper insight in analog design for both the novice as well as the experts. Finally, some “tricks” will be shown to outsmart practical noise or power limits.

Prof. Jurriaan Schmitz
(Univ. of Twente, Netherlands)

Jurriaan Schmitz was born in Elst, The Netherlands in 1967. He received his M.Sc. (1990, cum laude) and Ph.D. (1994) degrees in Experimental Physics at the University of Amsterdam on research carried out at the Nikhef research institute. In 1990 he was a CERN Summer Student. His research work was on new radiation detectors for tracking and energy measurement of high-energy particles.

After his Ph.D. he joined Philips Research as a Senior Scientist (1994-2002), studying CMOS transistor scaling, characterization and reliability. He worked on CMOS transistors from the 0.25 μm to the 90-nm node, studying super-steep retrograde wells, halo (pocket) implants, shallow junctions, GeSi gates, gate depletion and gate-last fabrication. Later he concentrated on characterization and reliability of CMOS devices, and studied the measurement issues arising from excessive gate leakage. He proposed the RF-CV characterization technique.

In 2002 he became full professor at the University of Twente as the successor of Prof. Hans Wallinga. He expanded his research interests to include above-IC technologies and light-from-silicon. With his coworkers and PhD students he worked on a variety of topics such as energy harvesting microchips, radiation imaging detectors on CMOS, and RF-CMOS and RF-MEMS reliability. He currently heads a research group of 20 people and supervises 10 Ph.D. students.

He has contributed to the organization of many IEEE conferences, in particular IEDM (where he was European Arrangements co-chair in 2012 and 2013) and ICMTS (being Technical Chair in 2008 and General Chair in 2011). He acts as Editor of IEEE Electron Device Letters and is an Editorial Advisory Board member of Solid-State Electronics. Prof. Schmitz authored or co-authored over 200 journal and conference papers, 18 patents, and three book chapters.

Abstract

Steep-slope transistor concepts for low-power CMOS

This tutorial will first quantify the main sources of power consumption in contemporary CMOS digital logic. Off-state leakage has emerged as the key bottleneck for the further improvement of power efficiency in CMOS circuits. This has inspired researchers to develop a zoo of new device concepts with extremely low off-state leakage current. These device concepts are classified in the tutorial and reviewed for their potential to revolutionize the integrated circuit. In particular, nano-electromechanical switches, tunnel transistors and devices based on piezo-electric action are discussed.

Invited Speakers

Prof. Sorin Cristoloveanu
(INPG, France)

Sorin Cristoloveanu received the PhD (1976) in Electronics and the French Doctorat ès-Sciences in Physics (1981) from Grenoble Polytechnic Institute, France. He is currently Director of Research CNRS. He also worked at JPL (Pasadena), Motorola (Phoenix), and the Universities of Maryland, Florida, Vanderbilt, Western Australia, and Kyungpook (World Class University project). He served as the director of the LPCS Laboratory and the Center for Advanced Projects in Microelectronics, initial seed of Minatec center. He authored more than 1,100 technical journal papers and communications at international conferences (including 160 invited contributions). He is the author or the editor of 28 books, and he has organized 25 international conferences. His expertise is in the area of the electrical characterization and modeling of semiconductor materials and devices, with special interest for silicon-on-insulator structures. He has supervised more than 80 PhD completions. With his students, he has received 13 Best Paper Awards, an Academy of Science Award (1995), and the Electronics Division Award of the Electrochemical Society (2002). He is a Fellow of IEEE, a Fellow of the Electrochemical Society, and Editor of Solid-State Electronics.

Abstract

Sharp switching devices based on band modulation

Recently proposed feedback-FETs with 'band modulation' schemes are conceptually different from MOSFETs or TFETs. They have similar gated-diode configuration as TFETs, but are operated in forward-bias mode. Electrostatic barriers are formed (via gate disposition and biasing) to prevent electron/hole injection into the channel until the gate or drain bias reaches a turn-on value. Due to band modulation along the channel and positive feedback mechanism, the device switches abruptly (< 1 mV/decade) from OFF state with low leakage current to ON state with high drive current.

The family of feedback barrier-modulation devices includes several SOI designs:

- Field-effect diode (FED) with two adjacent top gates,
- Thyristor-like structure with specific body doping partition and control via ground-plane bias,
- Z^2-FET (zero swing and zero impact ionization FET) which has an underlapped top gate and additional control from the ground plane.
- Z^3-FET (zero gate, zero swing and zero ionization) with free surface and controlled by two ground planes.

We will discuss in detail the device physics, architecture, and applications for the most promising variants (Z^2-FET and Z^3-FET). They feature a large hysteresis useful for single-transistor DRAM and SRAM cells, fast logic, ESD protection and sensing.

Invited Speakers

Dr. Seok-Hee Lee
(SK Hynix, Korea)

Executive Vice President and DRAM Chief Operating Officer, SK Hynix

Dr. Seok-Hee Lee received the B.S. and M.S. degrees from Seoul National University, Seoul, Korea, in 1988 and 1990, respectively, and the Ph.D. degree from Stanford University, Stanford, CA, in 2000 all in Materials Science.

From 2000 to 2010, he was with the Portland Technology Development, Intel Corporation, Hillsboro, OR, where he worked on process integration and yield on Intel's advanced CMOS logic technologies. Dr. Lee received the Intel Achievement Award three times (Intel's highest recognition for technical achievement) and 11 Intel divisional recognition awards for his technical achievements in transistor and process development. From 2010 to 2013, he was with the faculty of the Department of Electrical Engineering in KAIST, Korea, as an Associate Professor. In 2013, he joined SK Hynix as Senior Vice President and Head of R&D.

He is now Executive Vice President, responsible for DRAM products and technology. He served IEDM as a committee member and an executive committee member from 2008 to 2013.

Abstract

Technology Challenges and Opportunities of Mobile Memory

Semiconductor memory has been one of the most critical components of all computing systems for decades. At the same time, it has been considered a fundamental bottleneck in such systems in terms of performance. Breakthroughs in memory devices have accompanied two axes of microelectronics industry (PC and mobile), and the mobile era is still growing to date. Also, IoT is recently leading the other trend of growing market in mobile era.

Although technology scaling has improved density, power consumption, and performance, innovative technology in memory devices is continuously required for the power budget limitation in mobile systems.

This paper introduces memory technology to overcome scaling challenges of current and emerging memory devices along with promising solutions for low power.

Invited Speakers

Prof. Shinichi Takagi
(Univ. of Tokyo, Japan)

Shinichi Takagi was born in Tokyo, Japan, on August 25, 1959. He received the B.S., M.S. and Ph.D. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1982, 1984 and 1987, respectively. He joined the Toshiba Research and Development Center, Kawasaki, Japan, in 1987, where he has been engaged in the research on the device physics of Si MOSFETs. From 1993 to 1995, he was a Visiting Scholar at Stanford University, Stanford, CA, where he studied the Si/SiGe hetero-structure devices. He worked for the MIRAI Project as the leader of New Transistor Structures and Measurement/Analysis Technology Group from 2001 to 2007. In October 2003, he moved to the University of Tokyo, where he is currently working as a professor in the department of Electrical Engineering and Information Systems, School of Engineering.

Abstract

Non-Si MOSFET and TFET for low-power circuits

CMOS utilizing high mobility Ge/III-V channels on Si substrates is expected to be one of the promising devices for high performance and low power integrated systems in the future technology nodes, because of the enhanced carrier transport properties. In addition, Tunneling-FETs (TFETs) using Ge/III-V materials are regarded as one of the most important steep slope devices for the ultra-low power applications.

In this lecture, I would like to introduce the current status and future prospects of these non-Si material-based MOSFETs and TFETs on the Si CMOS platform for future ultra-low power integrated logic circuits with an emphasis on fundamental aspects of these semiconductor materials. The present technical challenges of the non-Si MOSFETs and TFETs will be summarized on a basis of the understanding of the device operation. In addition, possible and viable technological solutions for the above critical issues including gate stacks, source/drain formation and non-Si material integration with Si will also be addressed.

Invited Speakers

Prof. Byung-Gook Park
(Seoul National Univ., Korea)

Byung-Gook Park received his B.S. and M.S. degrees in Electronics Engineering from Seoul National University (SNU) in 1982 and 1984, respectively, and his Ph. D. degree in Electrical Engineering from Stanford University in 1990. From 1990 to 1993, he worked at the AT&T Bell Laboratories. From 1993 to 1994, he was with Texas Instruments. In 1994, he joined SNU as an assistant professor in the Department of Electrical and Computer Engineering, where he is currently a professor.

His current research interests include the design and fabrication of neuromorphic devices and circuits, flash memories, and silicon quantum devices. He has authored and co-authored over 1100 research papers in journals and conferences, and currently holds 101 Korean and 39 U.S. patents. He has served as a committee member on numerous international conferences, including Microprocesses and Nanotechnology, IEEE International Electron Devices Meeting, International Conference on Solid State Devices and Materials, Silicon Nanoelectronics Workshop (technical program chair in 2005, general chair in 2007), and International Technology Conference on Circuits, Systems, Computers and Communications (technical program chair in 2007, general chair in 2011). He served as an editor of IEEE Electron Device Letters and the editor-in-chief of Journal of Semiconductor Technology and Science. He served as the Seoul Section chair of IEEE (2014) and the president of Institute of Electronics and Information Engineers (2015). He received “Best Teacher” Award from SoEE in 1997, Doyeon Award for Creative Research from ISRC in 2003, and Educational Award from College of Engineering, SNU, in 2006, Haedong Research Award from IEEK in 2008, and Best Research Award from SNU in 2015.

Abstract

Synaptic Devices and Neuron Circuits for Neuromorphic Chips

In order to achieve the efficiency of biological neural system, we have to develop the building blocks (synaptic devices and neuron circuits) of spiking neural networks (SNNs). In this talk, we will review and discuss various approaches to implement the basic building blocks for neuromorphic chips. Starting from the description of biological building blocks (neurons and synapses) and their learning mechanism, we will briefly review the software approaches to imitate the functions of biological neural system. In this process, we will find that the success of artificial neural networks (ANNs) critically depends on how closely we can imitate the biological system and that SNNs with STDP learning mechanism are the best candidate for neuromorphic chip implementation. Various memory devices such as flash memory, resistive memory, phase change memory, and magnetic tunnel junction memory have been proposed as synaptic devices. They are compared in terms of energy consumption and multi-level operation. As neuron circuits, there have been both digital and analog circuit approaches. Since the biological neural network is an analog system, we will focus on the analog circuit approaches. Integrate-and-fire (I&F) circuits can emulate a neuron efficiently, and we can implement spike-timing-dependent plasticity (STDP) using a feedback signal with asymmetry in time.

Invited Speakers

Prof. Debdeep Jena
(Cornell Univ., USA)

Debdeep Jena received the B. Tech. degree with a major in Electrical Engineering and a minor in Physics from the Indian Institute of Technology (IIT) Kanpur in 1998, and the Ph.D. degree in Electrical and Computer Engineering at the University of California, Santa Barbara (UCSB) in 2003. His research and teaching interests are in the MBE growth and device applications of quantum semiconductorheterostructures (currently III-V nitride semiconductors), investigation of charge transport in nanostructured semiconducting materials such as graphene, nanowires and nanocrystals, and their device applications, and in the theory of charge, heat, and spin transport in nanomaterials. He is the author on several journal publications, including articles in Science, Physical Review Letters, and Electron Device Letters among others. He has received two best student paper awards in 2000 and 2002 for his Ph.D. dissertation research, the NSF CAREER award in 2007, and the Joyce award for excellence in undergraduate teaching in 2010.

Abstract

Taking Gallium Nitride HEMTs into the THz

The III-Nitride semiconductor family comprising GaN, InN, and AlN and their heterostructures has emerged as very attractive for RF applications because one can apply much higher drain voltages without breaking down the device – thus allowing for higher RF power amplification, which goes simply as ~Imax x Vmax, the current and voltage handling capability of each transistor. Because of high-density polarization-induced 2D electron gases, the current drives in GaN HEMTs are approaching ~3-4 mA/um, higher than any other semiconductor technology. Because of the large bandgap, the breakdown voltage is high, and thus the RF power obtained from GaN HEMTs far exceeds any other semiconductor technology at a given frequency. However, GaN HEMTs currently seem to have hit a speed limit of ~0.4 – 0.5 THz, as recently demonstrated by us and other groups. While this was inconceivable ~10 years ago and is quite a significant achievement by itself, it remains quite a bit lower than InP technology. In my presentation, I will discuss what made the technology possible in GaN – by digging all the way down to fundamental carrier transport properties and scaling, quasi-ballistic transport, MBE regrown contacts, innovations in gate stack engineering, etc.

For further progress towards a viable THz electronics technology with the III-nitrides, one must improve the speed – to compete with InP, and to potentially enable much higher power levels because of the high breakdown. However, this may require some fundamental breakthroughs in the device design, and may or may not happen. It will for sure not happen if we do not explore! To that end, I will share some new ideas – such as k-space engineering and isotope engineering, and potentially exploiting interband tunneling and topological properties that emerge when the high polarization fields that result from the broken symmetry in the III-Nitride crystals are coupled in certain ways with quantum heterostructure design. I will share some preliminary experimental efforts from my group heading in that direction.

Invited Speakers

Prof. Tibor Grasser
(Technical Univ. of Vienna, Austria)

Prof. Tibor Grasser received the Diplomingenieur degree in communications engineering, the Ph.D. degree in technical sciences, and the venia docendi in microelectronics from the Technische Universität Wien in 1995, 1999, and 2002, respectively. He is currently the Head of the Institute for Microelectronics at TU Wien. Since 1997 he has headed the Minimos-NT development group, working on the successor of the highly successful MiniMOS program. From 2003 till 2010 he was the director of the Christian Doppler Laboratory for TCAD in Microelectronics. Prof. Grasser is the co-author or author of over 500 articles in scientific books, journals, and conferences proceedings, and has presented invited talks, tutorials and short courses at various conferences such as the IEDM, IRPS, VLSI Symp., SISPAD, ESSDERC, IIRW, ESREF, INFOS, ISDRS, and the ECS meetings. He is an IEEE Fellow, the editor of a book on advanced device simulation, organic electronics, the bias temperature instability, and hot carrier degradation, a distinguished lecturer of the IEEE Electron Devices Society, has been involved in the program and management committees of conferences such as IEDM, IRPS, SISPAD, IWCE, ESSDERC, IIRW, and ISDRS, and is a recipient of the Best Paper Awards at IRPS (2008, 2010, and 2012), ESREF 2008, and IPFA (2013 and 2014) as well as the IEEE EDS Paul Rappaport Award 2011. He was also a Chairman of SISPAD 2007 and General Chair of IIRW 2014. His current scientific interests include semiconductor device reliability issues as well as device modeling and simulation in general. He currently serves as an Associate Editor for Microelectronics Reliability (Elsevier).

Abstract

Charge Trapping and Time-dependent Variability in Low-Voltage MOS Transistors

Charge trapping in the insulating oxide of MOS transistors has been linked to a number of detrimental issues, like random telegraph and 1/f noise, and bias temperature instabilities. With the rapid scaling of modern devices these phenomena are becoming more and more important. Although nanoscale devices only contain a small number of defects, each of them can have an increasingly catastrophic impact on the overall device behavior. In particular, dynamic changes in the occupancy of these defects which occur particularly often at low operating voltage lead to time-dependent variability, which becomes more and more important as device sizes are further reduced. With the recently developed time-dependent defect spectroscopy (TDDS), the capture and emission of single carriers can be studied. The latest TDDS results will be reviewed together with their implications on modeling and reliability predictions. Furthermore, it will be shown how the charge trapping in the oxide leads to long term device degradation, typically referred to as bias temperature instability. In particular, I will summarize recent results which show that device degradation at low voltages is poorly reflected by main-stream models and discuss our recently suggested hydrogen-release model which covers these effects.

Invited Speakers

Dr. Maryse Fournier
(LETI, France)

Maryse Fournier is a Process Integration Engineer at CEA-LETI. She graduated from the Conservatoire National des Arts et Métiers of Grenoble in 1993. She has been working for 10 years in Sofradir Company where she was in charge of the flip-chip assembly of infrared focal planes. In 2000, she joined CEA-LETI to develop processes and electro-optical characterizations of advanced infrared detectors. Since 2010, she is working in the 200mm CMOS foundry to develop devices for Silicon Photonics applications. She is in charge of the Multi Project Wafer operations within LETI, under FP7-PHOTONFAB and FP7-ESSenTIAL projects for the European ePIXfab platform. She is also involved in various European funded FP projects (FAON, FABULOUS, IRIS) and industrial collaborations. She is co-author of more than 30 papers in journals and conference proceedings in its field of expertise.

Abstract

Photonics on CMOS is Key Enabling Technology for innovation

Photonics technologies are emerging as very attractive for a wide range of industrial, environmental and scientific applications. Integrated Optics devices and systems are key solutions to solve current limitations, such as lower power consumption, low cost, small footprint, ultra-high bandwidth. They are addressing some challenges that have no equivalent in electronic domain. The well-established and compatible CMOS fabrication platform had allowed considerable development to require flexibility, high integration, high functionality, multiplexed and 3D solutions. We raise challenges and find novel solutions to merge Photonics Integration Circuit and electronic circuits on 3-D chip assemblies.