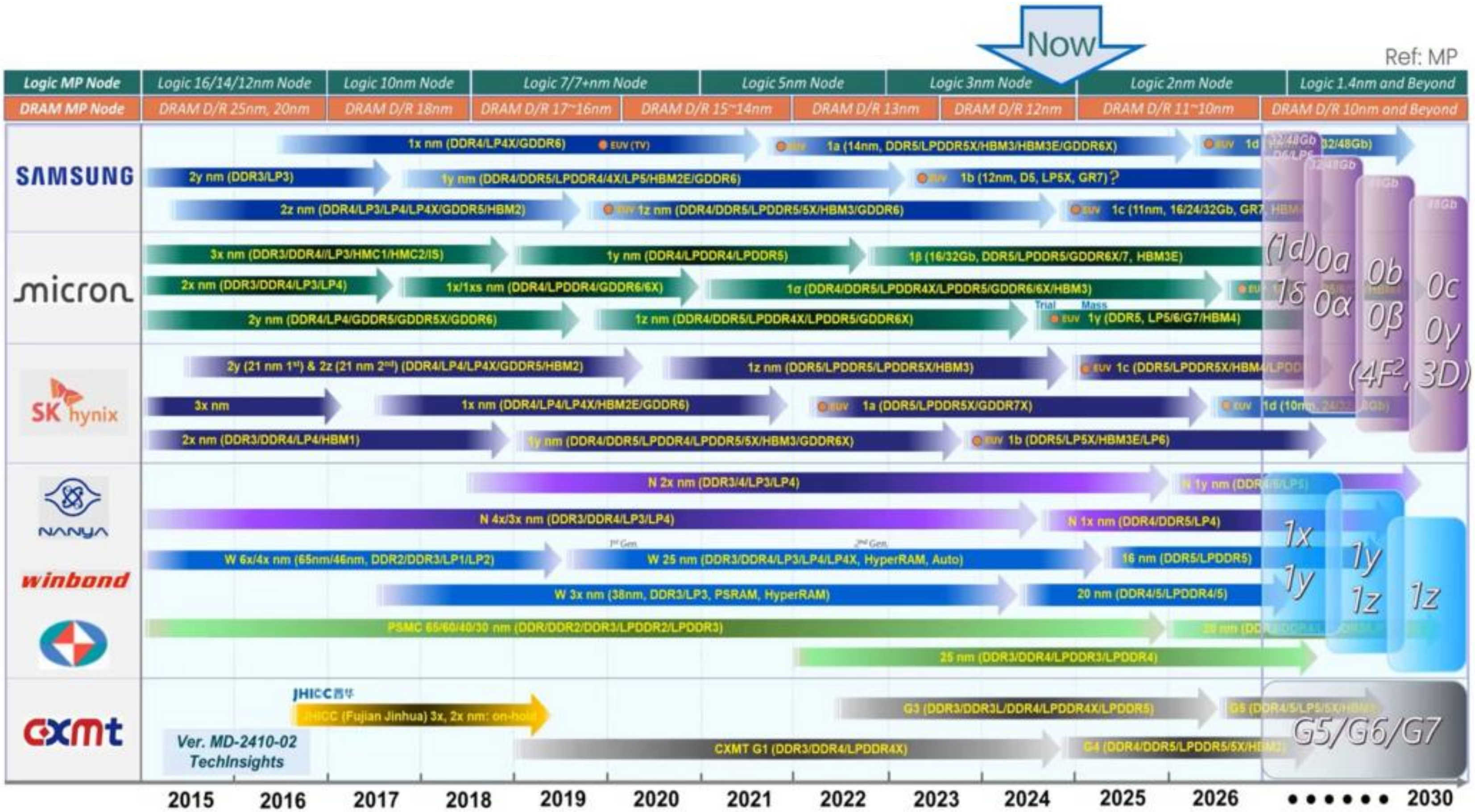
# ADVANCED NANO-DEVICE TECHNOLOGY

## DRAM

# DRAM Technology Roadmap

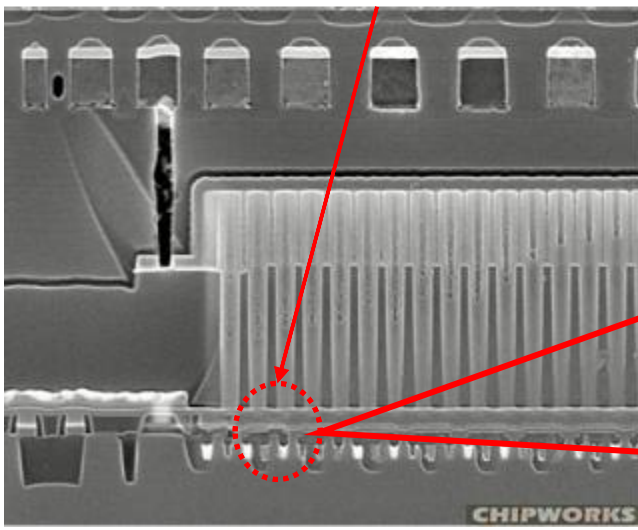


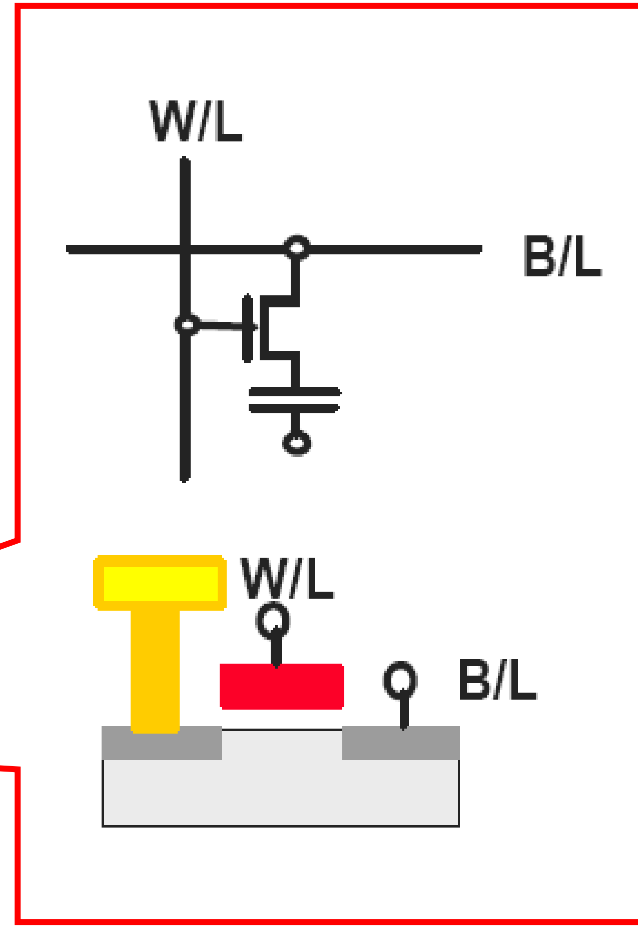

Tech Insights

1 

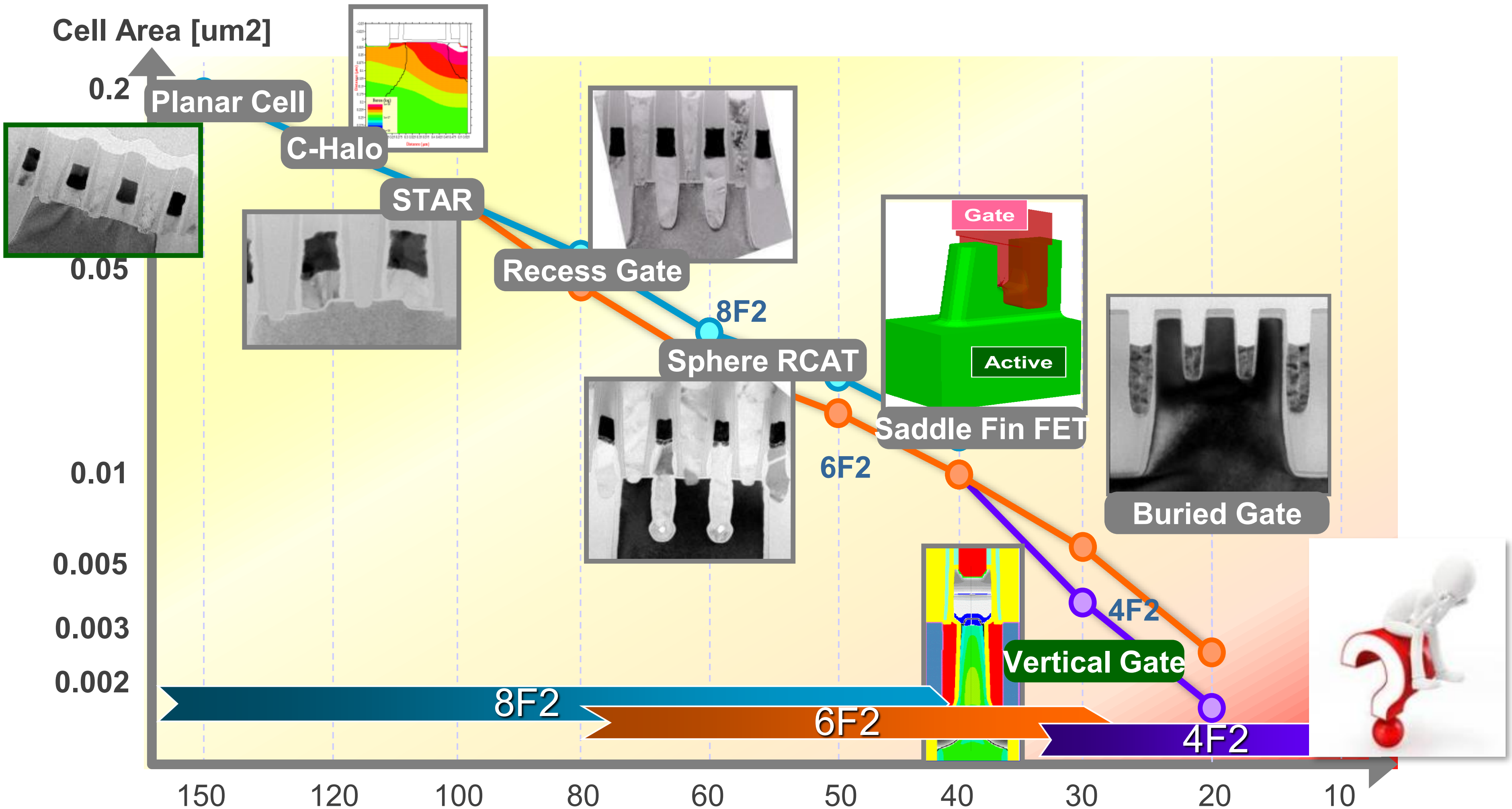
# 1T1C Memory Cell @ DRAM

## Structure



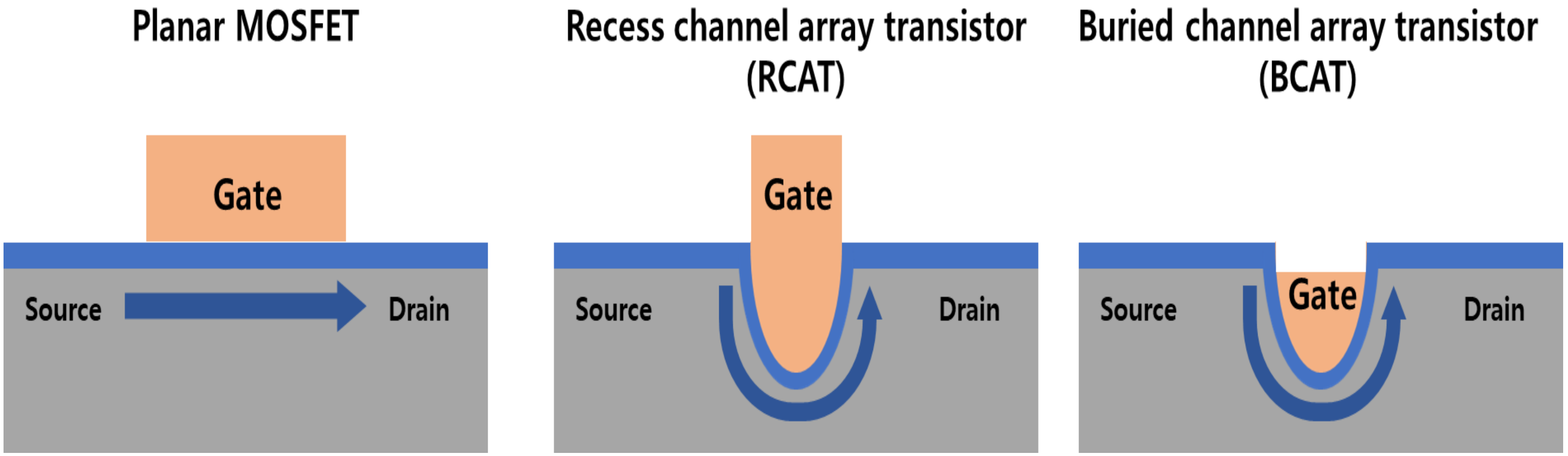



# Memory Cell Transistor Revolution




SK Hynix, IEDM17

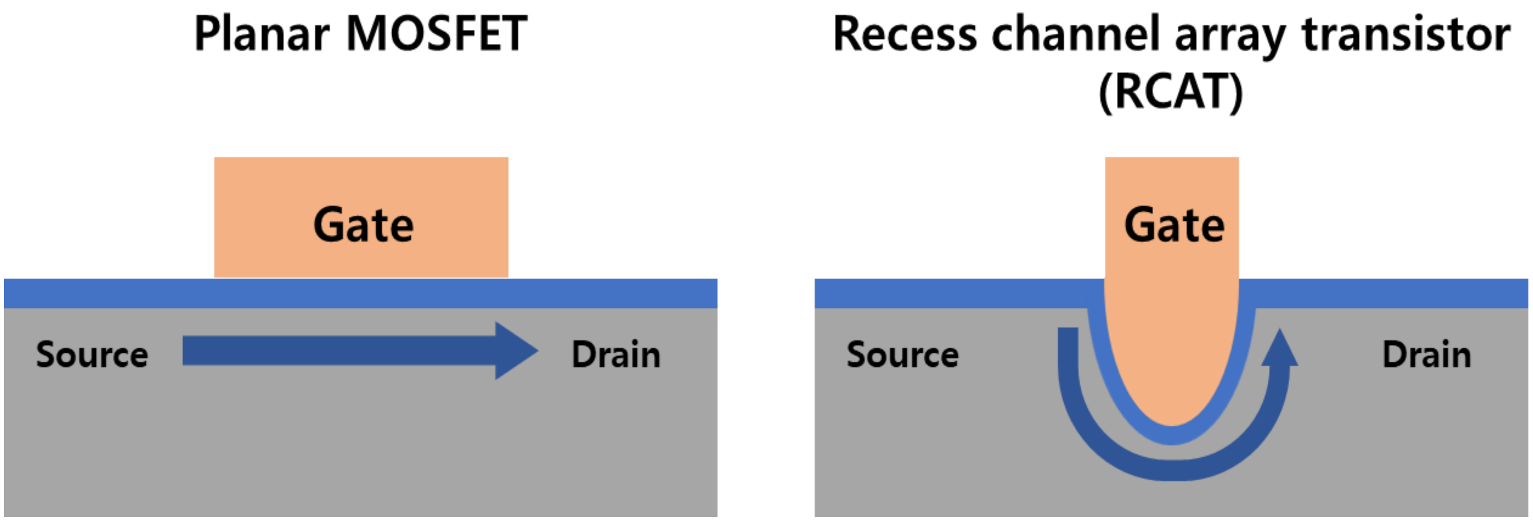
# Memory Cell Transistor Revolution




**Planar MOSFET → RCAT → BCAT**

# Recess Channel Array Transistor (RCAT)

- Why RCAT?




**Planar MOSFET: Scaling down 시 channel length 가 감소하며 short channel effect가 발생.**
**→ DIBL, HCI 등 발생하여, $V_T$ 및 off current 제어가 어려움.**

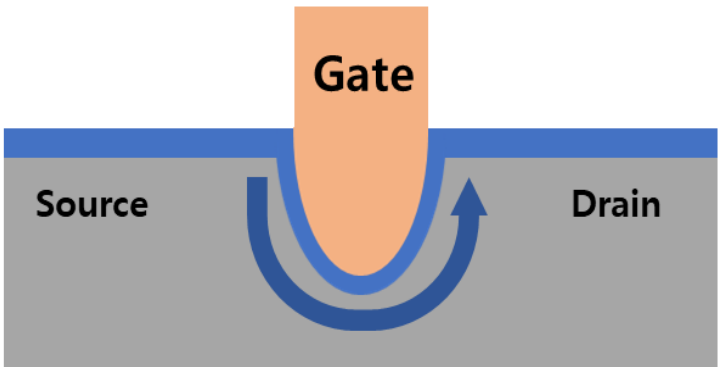
**RCAT: 채널을 recess 시켜 아래로 형성함으로써, 같은 집적도에서 긴 채널 길이를 확보할 수 있음.**
**→ Short channel effect 해소 가능.**

# Buried Channel Array Transistor (BCAT)

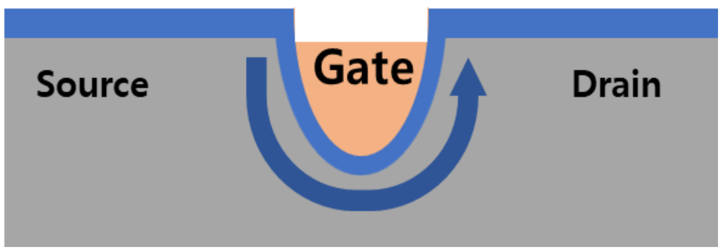
➢ Why BCAT?

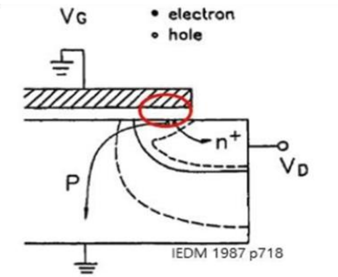
* GIDL

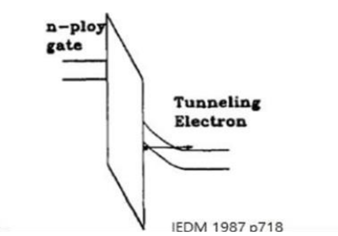
Recess channel array transistor (RCAT)




Buried channel array transistor (BCAT)




**BCAT:**
**게이트 전극의 상단을 매립하여, DRAM word line과 bit line 간의 간섭을 개선할 수 있음.**
**게이트 전극 매립 시, Gate와 Drain간 overlap되는 채널영역이 감소하여, GIDL 현상을 개선할 수 있음.**

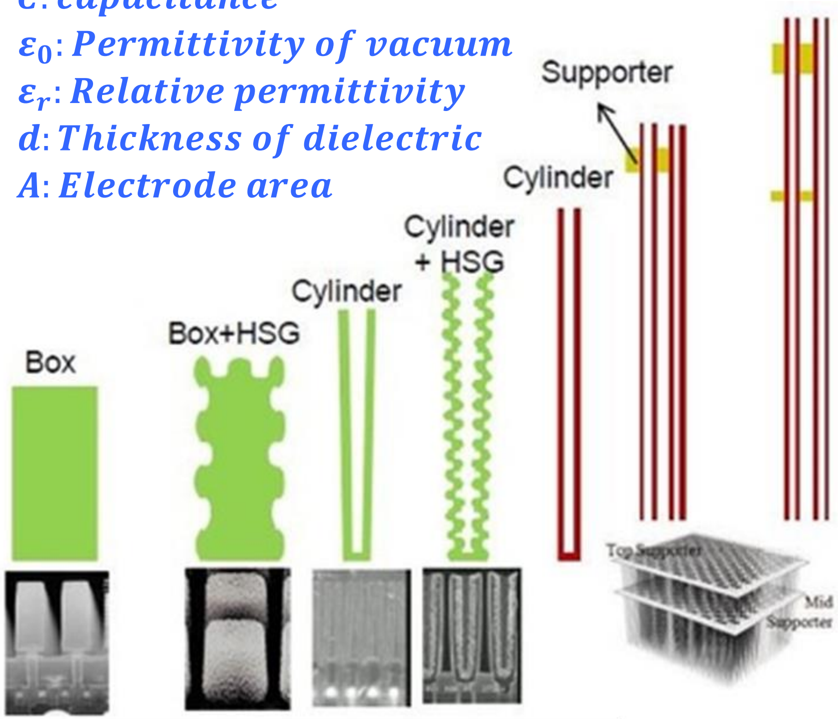
# DRAM Capacitor

**Planar → Concave → Cylinder → Pillar**

- Capacitance & history of capacitor scheme

$$C = \frac{\varepsilon_0 \varepsilon_r A}{d}$$

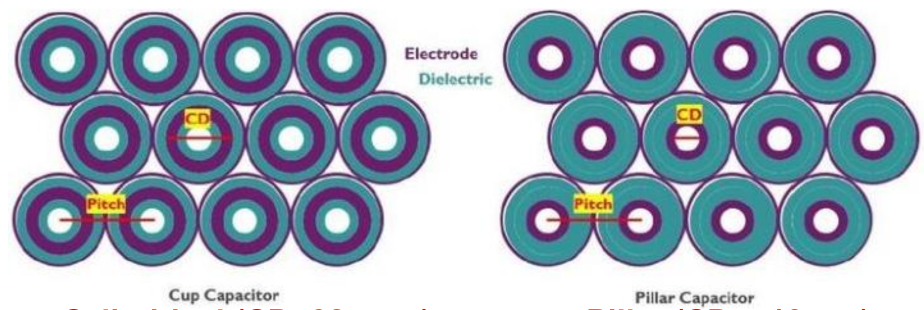
*$C$: capacitance*
*$\varepsilon_0$: Permittivity of vacuum*
*$\varepsilon_r$: Relative permittivity*
*$d$: Thickness of dielectric*
*$A$: Electrode area*




*Courtesy of IEDM 2018*

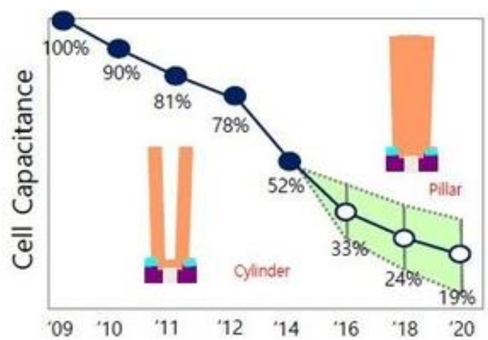
- Projected road map for DRAM capacitor

| Item | DRAM Node D18 Cylinder | DRAM Node D16 Cylinder | DRAM Node D16 Pillar | DRAM Node D14 Pillar | DRAM node D12 pillar |
|---|---|---|---|---|---|
| Capacitor specification | 10fF | 8fF | 8fF | 6fF | 6fF |
| Hole / pillar etch CD | 38nm | 32nm | 26nm | 19nm | 13nm |
| Hole / pillar hexagonal pitch | 56nm | 50nm | 50nm | 43nm | 37nm |

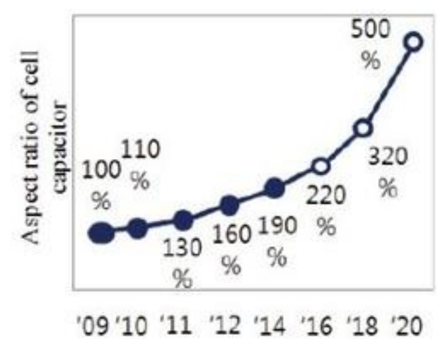



**Cylindrical (CD: 38 nm~)** **Pillar (CD: ~13 nm)**

- Capacitance reduction



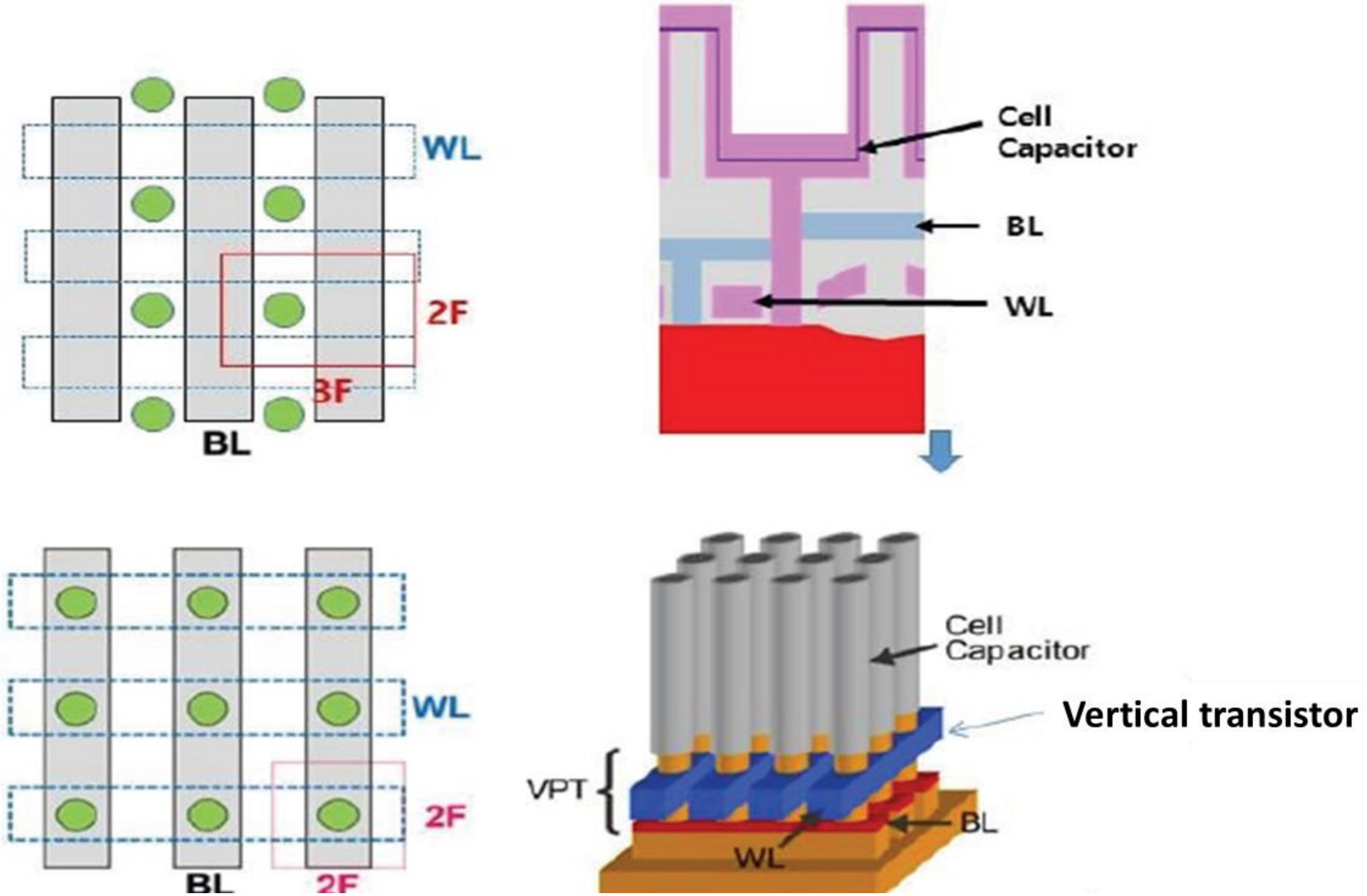

- Aspect ratio of capacitor




*Courtesy of IEDM 2018*

# $4F^2$ DRAM

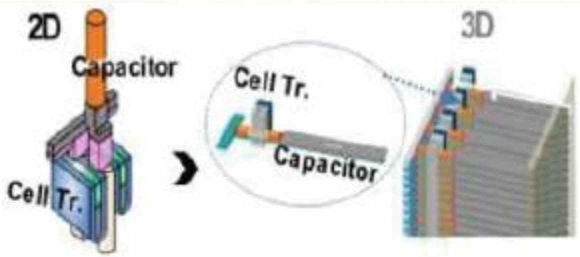
➢ **$4F^2$ DRAM : BCAT → Vertical transistor**




- By applying a vertical transistor, the feature size can be improved from $6F^2$ to $4F^2$.
- Currently, due to the extremely high complexity of 3D DRAM fabrication, $4F^2$ DRAM is planned for the next DRAM cell structure.

# 3D-DRAM (Samsung, VLSI 2023)

➢ **3D DRAM (Samsung, 2023 IEDM)**




iedm 2021 K. Kim (Samsung)

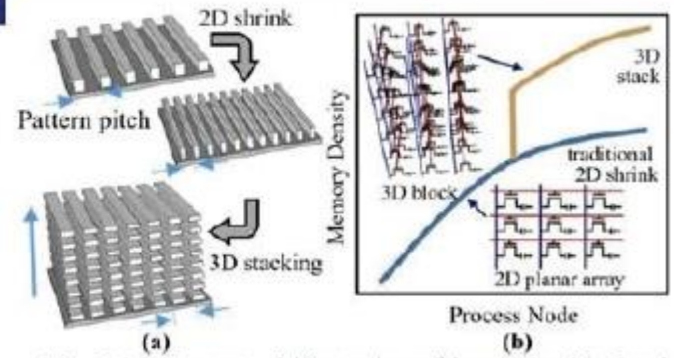



Fig. 2 (a) Conceptual illustration of increasing bit density by shrinking 2D patterns, then switching to 3D cubic block and (b) the scaling forecast by 3D stack.

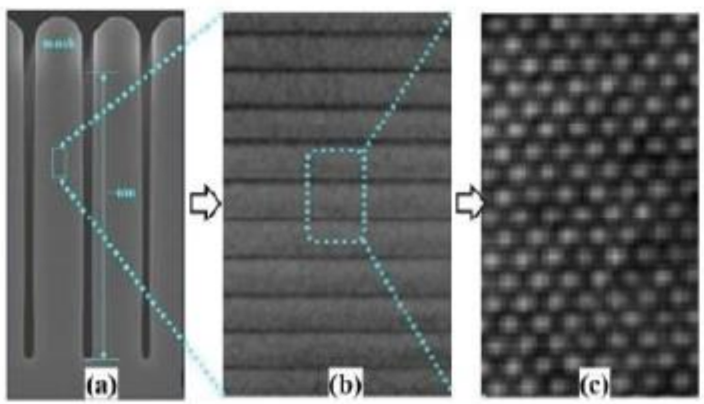



Fig. 3 TEM images of (a) multiple layered epitaxial stack of Si /SiGe layer, (b) zoom-in view, and (c) silicon lattice structure confirming single crystallinity.

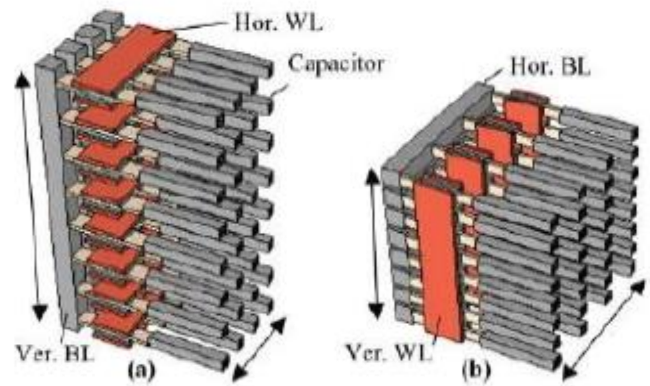



Fig. 4 Two possible orientations of control lines; (a) horizontal WL and (b) vertical WL. The choice lies between vertical or horizontal complexity. horizontal complexity.

- 3D DRAM: A design where capacitor is formed horizontally, enabling vertical stacking of DRAM cells.
- 3D DRAM requires highly complex process such as Si/SiGe epitaxial growth and selective etching.

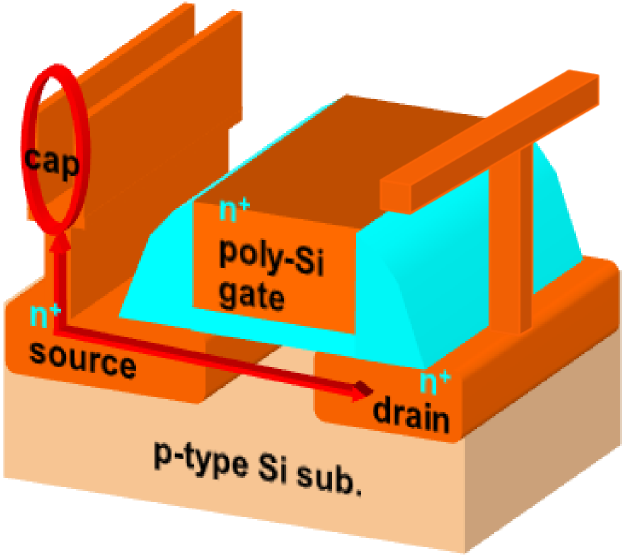
# ADVANCED NANO-DEVICE TECHNOLOGY

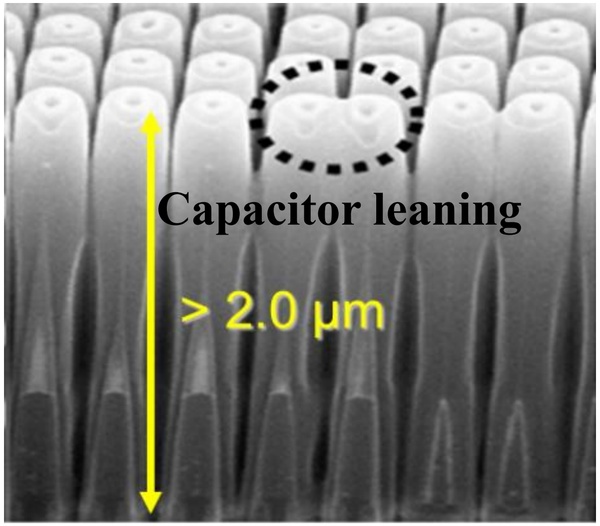
**(2025-1)**

# Emerging Memory
# (MRAM)

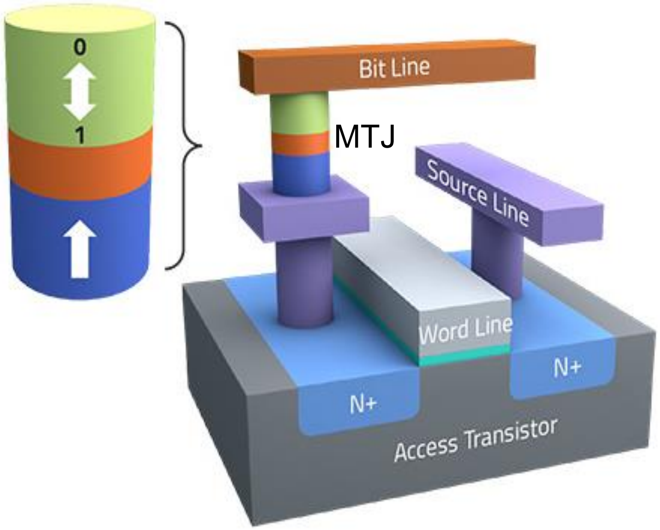
# DRAM의 Scaling Limitation

**DRAM cell : 1T1C**

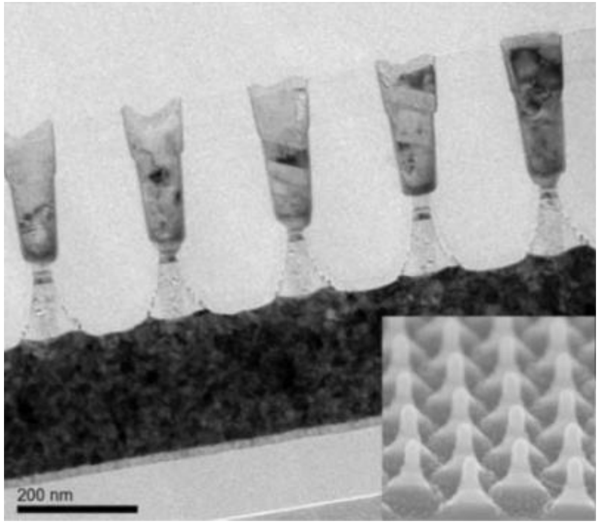



**MRAM cell : 1T1R**



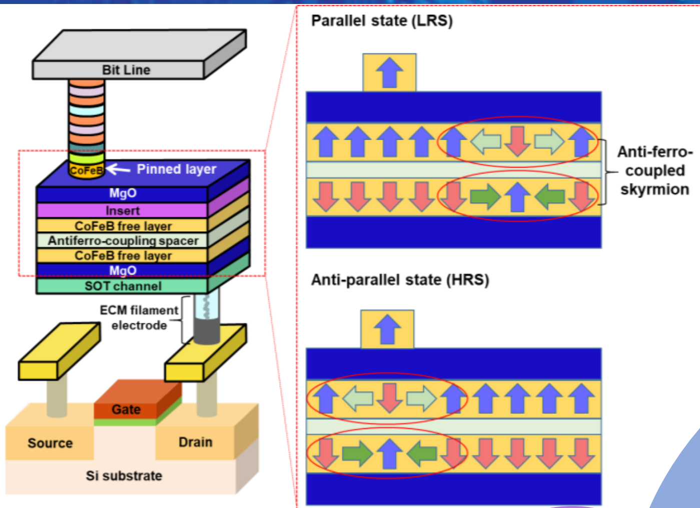

*SEMICONDUCTOR ENGINEERING

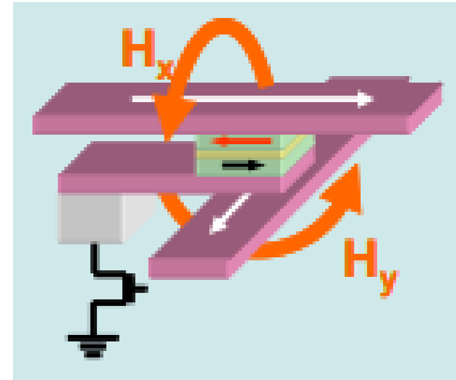


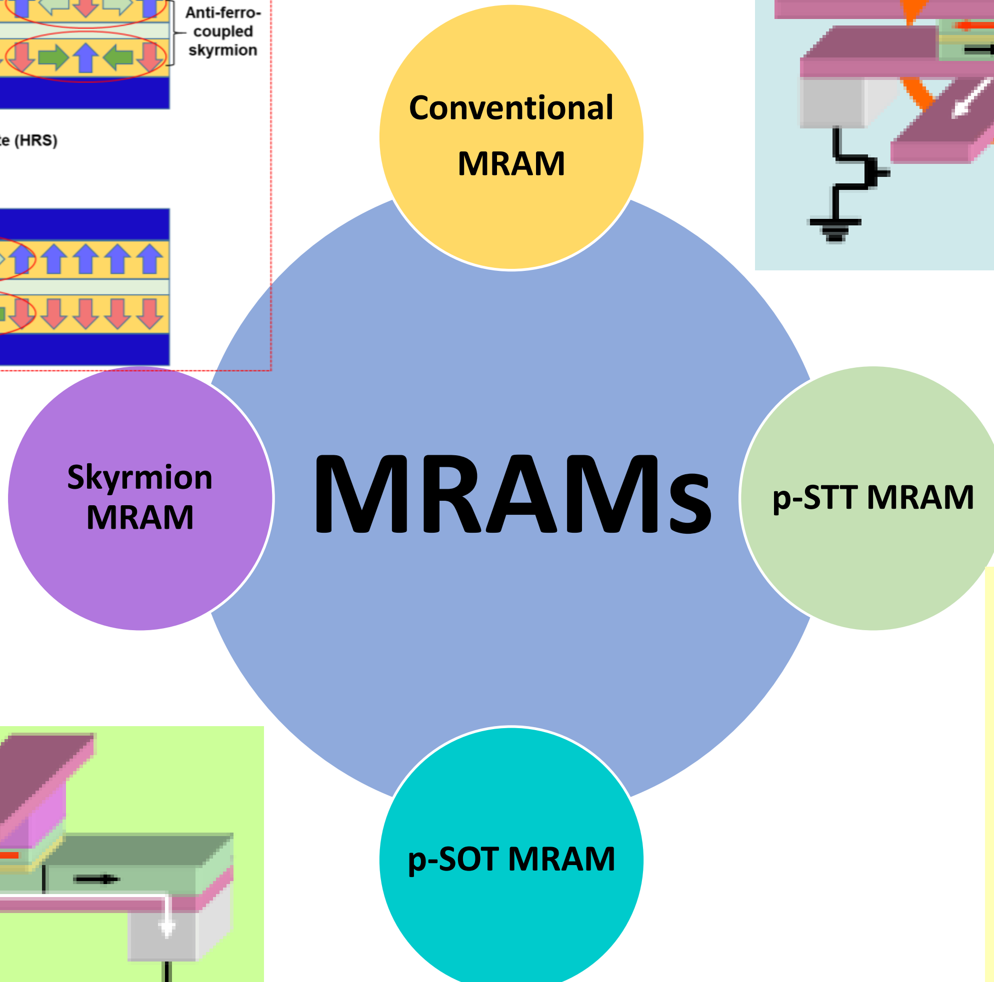
# Comparison of Emerging Memory

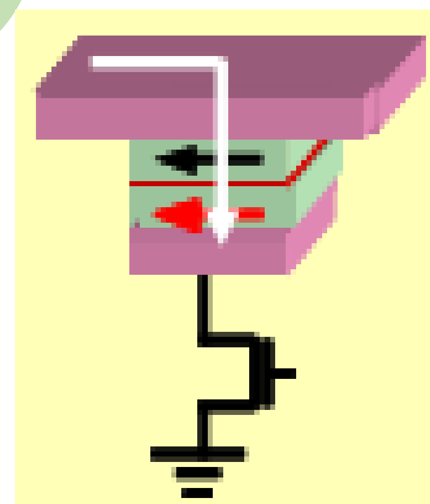
| Item | MRAM | FeRAM | PRAM | ReRAM | FLASH | SRAM | DRAM |
|---|---|---|---|---|---|---|---|
| Memory principle | Ferro magnet | Ferro Electric | Phase change film | Unknown | Floating gate | Transistor | Capacitor |
| Non-volatile | ○ | ○ | ○ | ○ | ○ | × | × |
| Endurance | Unlimited (>$10^{15}$) | Limited | Limited | Limited | Limited | Unlimited (>$10^{15}$) | Unlimited (>$10^{15}$) |
| Access speed | ◎ (<10 ns) | ○ | △ | ○ | ○(read) ×(write) | ◎ | ○ |
| Refresh operation | Unnecessary | Unnecessary | Unnecessary | Unnecessary | Unnecessary | Unnecessary | Necessary |
| Cell size | ○ or △ | ○ | ◎ | ◎ | ◎ | △ | ○ |
| Low power | ○ | ○ | ○ | ○ | △ | ○ | ○ |
| Thermal stability | ○ | × | × | Unknown | △ | ○ | △ |
| Application | Work memory | Work memory | Storage | Storage | Storage | Work memory | Work memory |

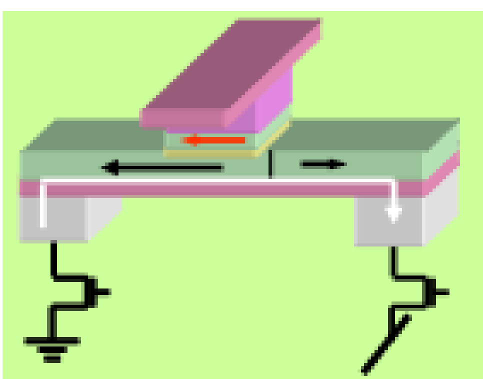
# Classification of MRAMs



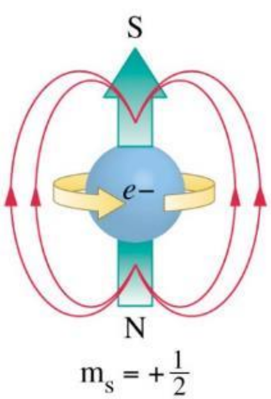


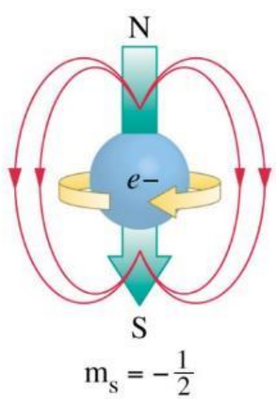
# Spin-transfer-torque MRAM (STT MRAM)

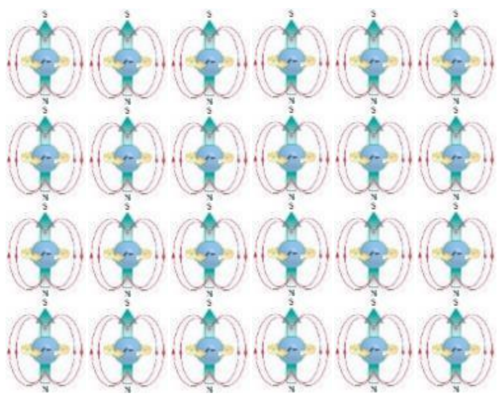
# Introduction

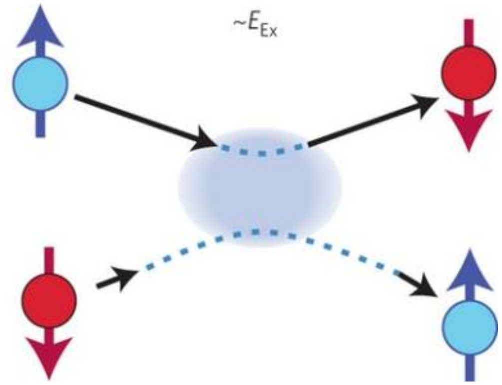
It is a fundamental fact that the macroscopic magnetization intensity of a magnet such as iron arises from the cooperative mutual alignment of elementary magnetic moments carried by electrons. An electron is little more than a mass particle carrying an electrostatic charge, which spins at a constant rate, like a planet about its axis. The electric current of this spin induces a surrounding magnetic field distribution resembling that which surrounds the Earth. Thus, each electron is effectively a miniscule permanent magnet. . .
: 물질 주위를 회전하는 전자는 극소량의 영구적인 자성을 띄게 하는데, 이러한 자기모멘트가 상호 정렬함으로써 자화 (magnetization intensity)가 형성된다.

. . . **The exchange interaction** is that force, arising quantum-mechanically from electrostatic interactions between spinning electrons, which causes this mutual alignment . . . Not only does it couple the bound spins of a ferromagnet to each other, but it also couples the spins of moving electrons, such as those partaking in current flow, to these bound electrons.
: **교환상호작용**은 회전하는 전자 간의 전기적 상호작용에 의한 힘으로, 강자성체 안의 전자 사이 뿐만 아니라 전류의 흐름에 의해 이동하는 전자와 강자성체 안의 전자 사이에도 발생한다.



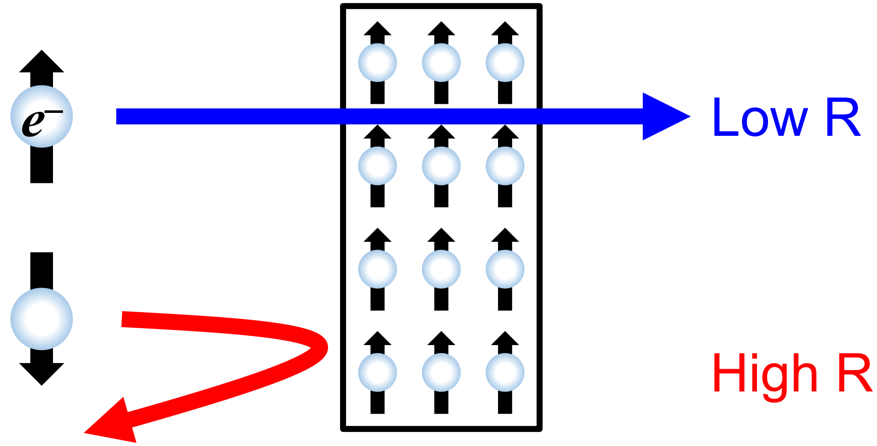



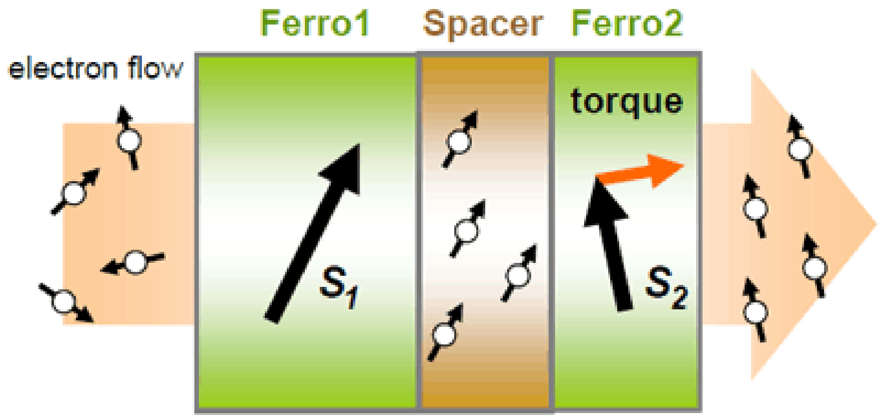





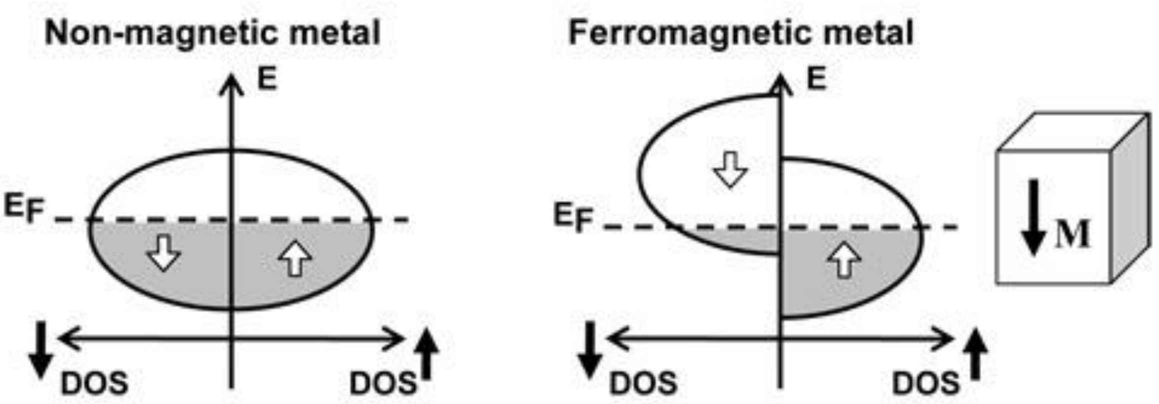
# Spin Polarization of Free Electrons in FMs

- **Spin-dependent scattering**



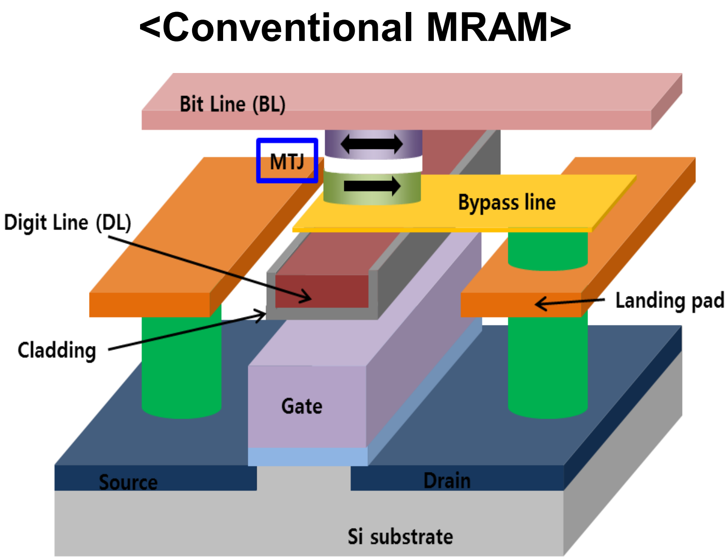

- **Spin polarization**

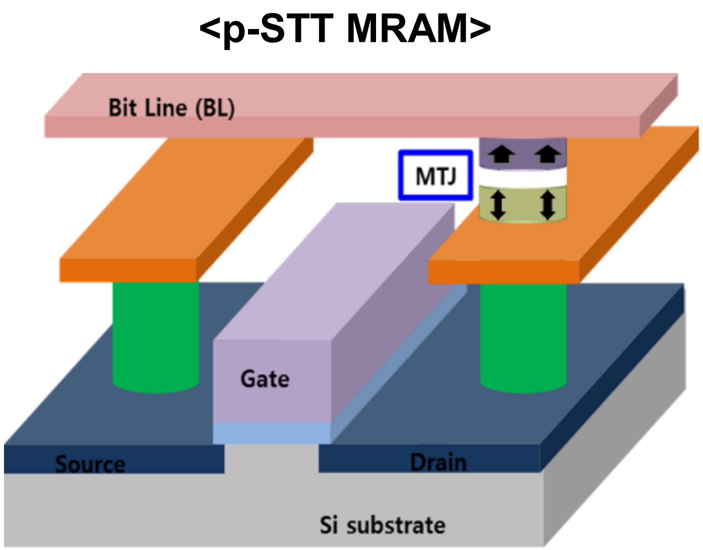


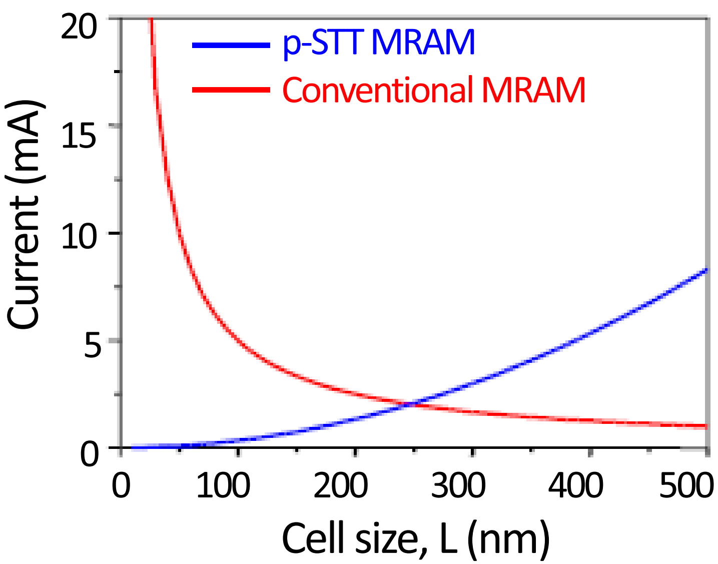

$$P = \frac{D_{\uparrow}(E) - D_{\downarrow}(E)}{D_{\uparrow}(E) + D_{\downarrow}(E)}$$

cf. Co : ~0.35
Fe : ~0.40
CoFeB : ~0.65

# Necessity of p-STT MRAM



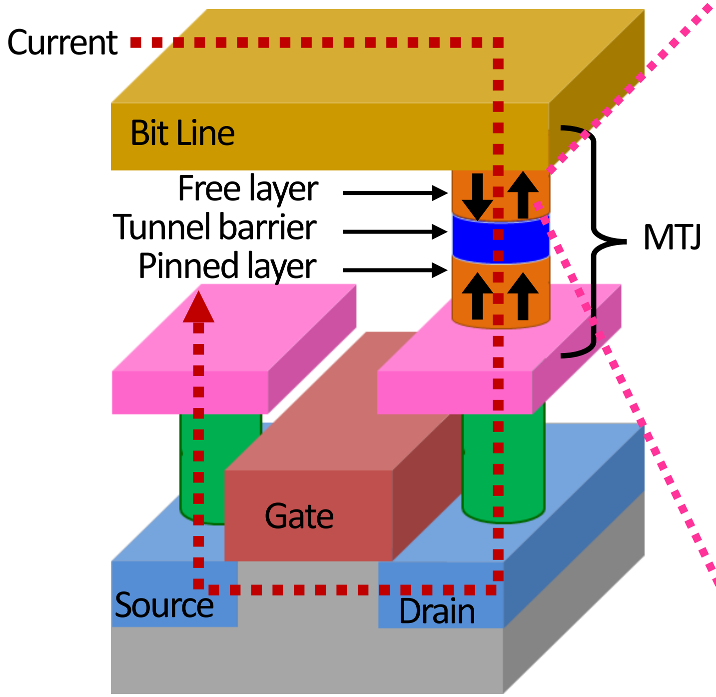




the incoming polarized electrons by the spin filter layer, FM1 exchange with FM2

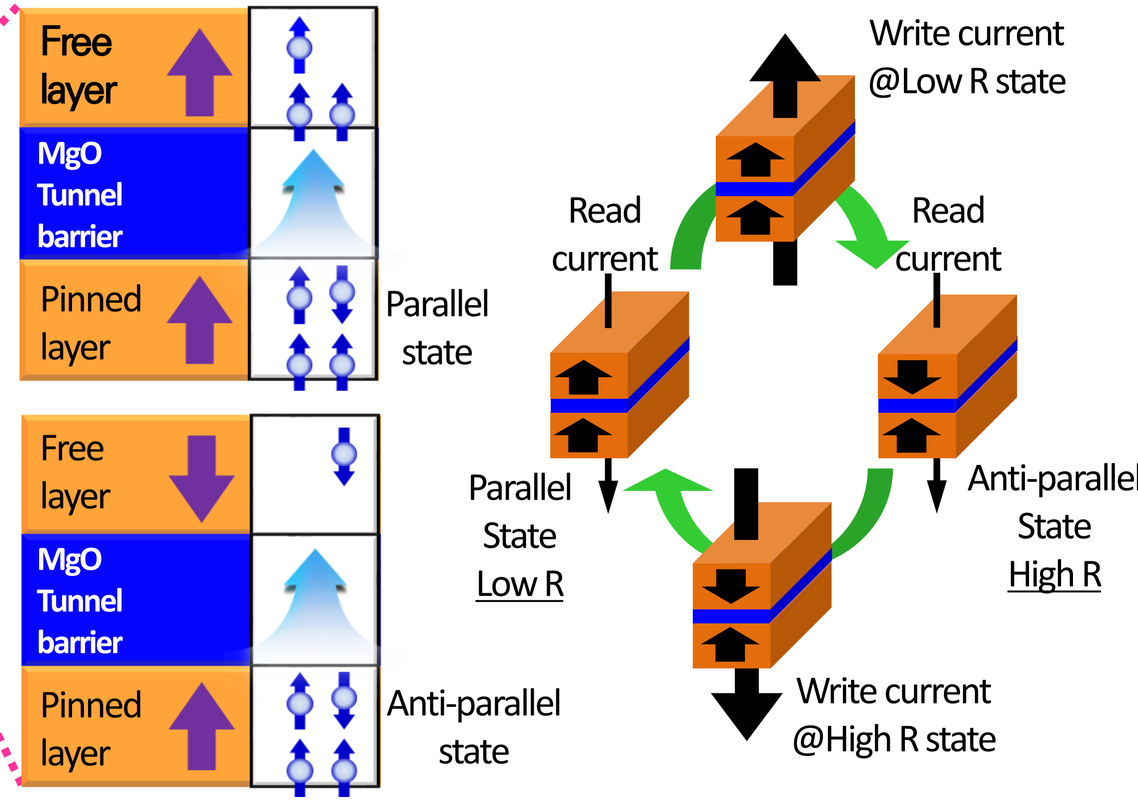
- **Bounded electrons in FM**
  **: polarizing the free electron (Spin filter)**
- **Free electrons in polarized current**
  **: switching magnetization . (STT switching)**

# p-STT MRAM cell의 기본 구조: 1T1R

## <p-STT MRAM cell>

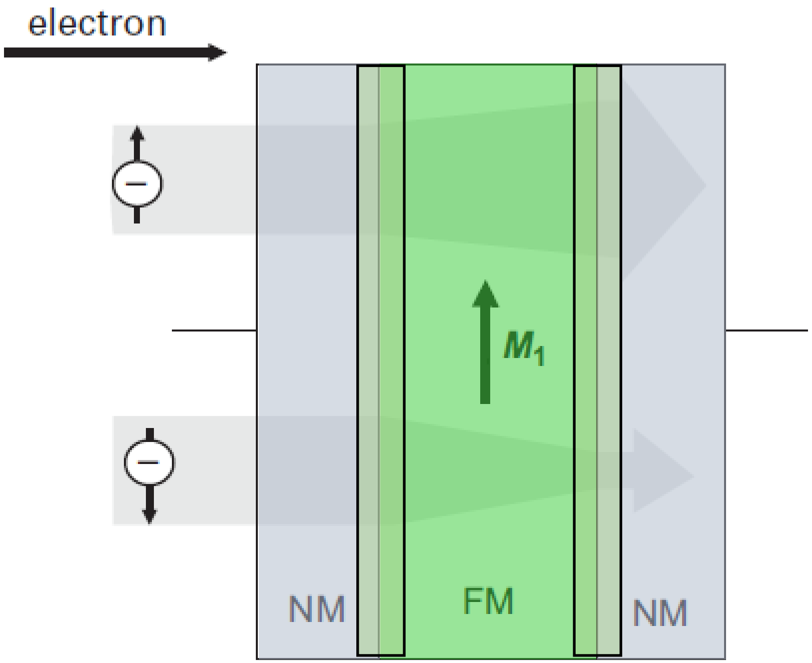



## <p-STT MRAM cell operation>



# Spin Polarization of Free Electrons in FMs

- **Spin filtering**




GMR effect of NM / FM / NM layers

| | Up spin | Down spin | Function |
|---|---|---|---|
| NM | Equally scattered | Equally scattered | Equal population of the two spins |
| Interface of FM and NM | Less scattered | More scattered | Spin filter depending on spin polarity |

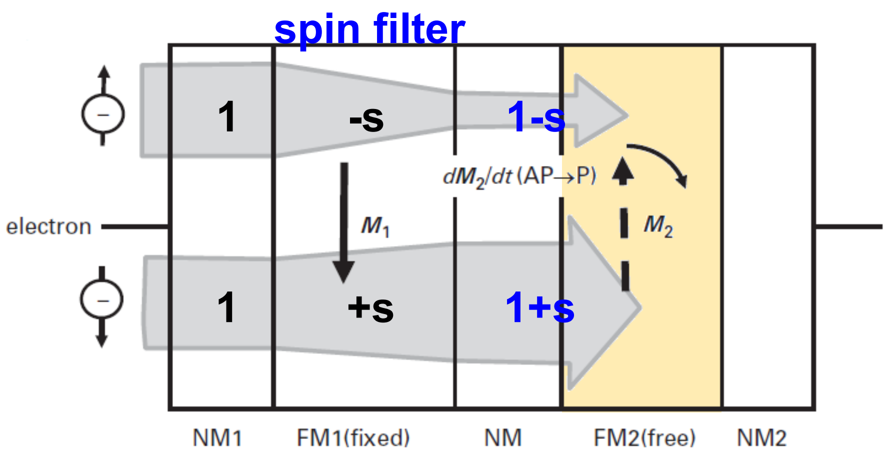
- **Bounded electrons in FM**
  : polarizing the free electron (Spin filter)
- **Free electrons in polarized current**
  : switching magnetization . (STT switching)

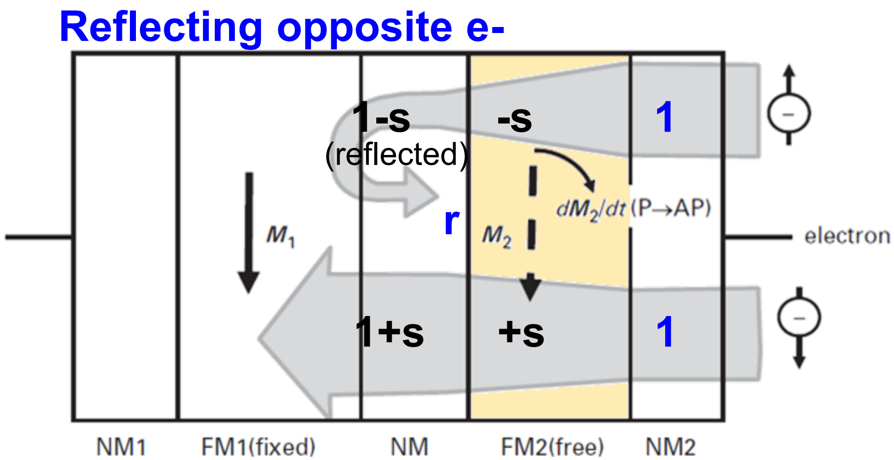
# STT in a Multilayer Thin-film Stack

- **Switching of resistance state**

**AP-> P**
**Spin filter**

**P -> AP**
**Reflection**




➡ the incoming polarized electrons by the spin filter layer, FM1 exchange with FM2

➡ Both the incoming and the reflected minority-polarized electrons exchange with FM2

# ADVANCED NANO-DEVICE TECHNOLOGY

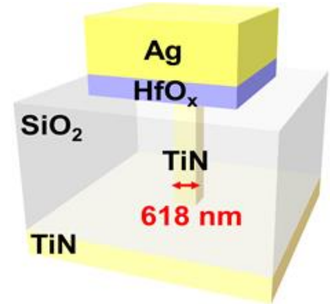
**(2025-1)**

## Emerging Memory
## (ReRAM)

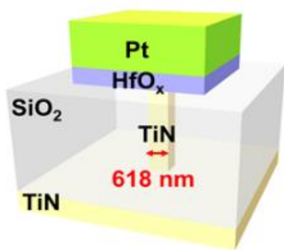
# Types of ReRAMs

**ReRAMs**

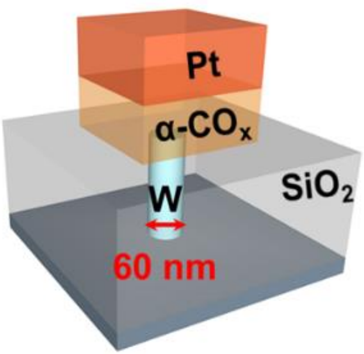
- **ECM** (Metal filament-type)



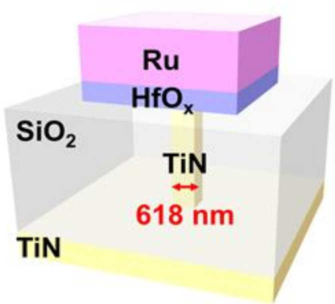

- **VCM** (Oxygen vacancy filament-type)

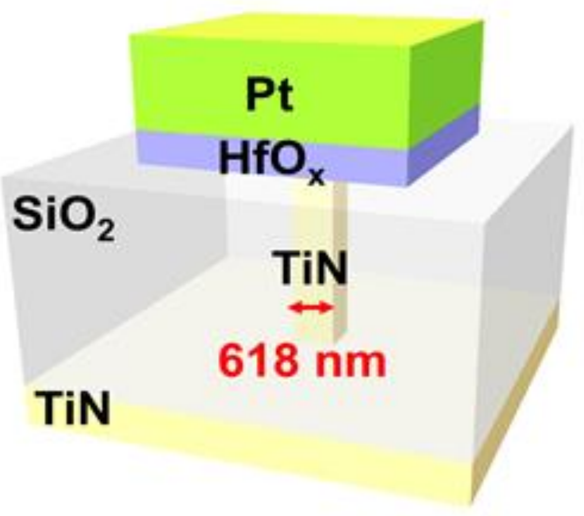


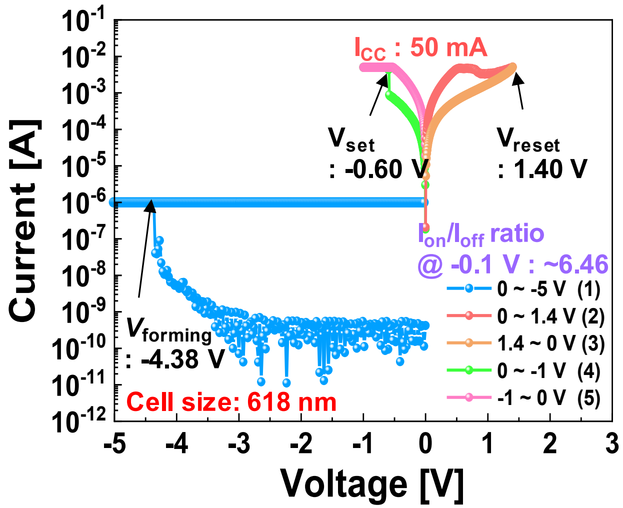

- **VCM** (Unique C-C $sp^2$ filament-type)

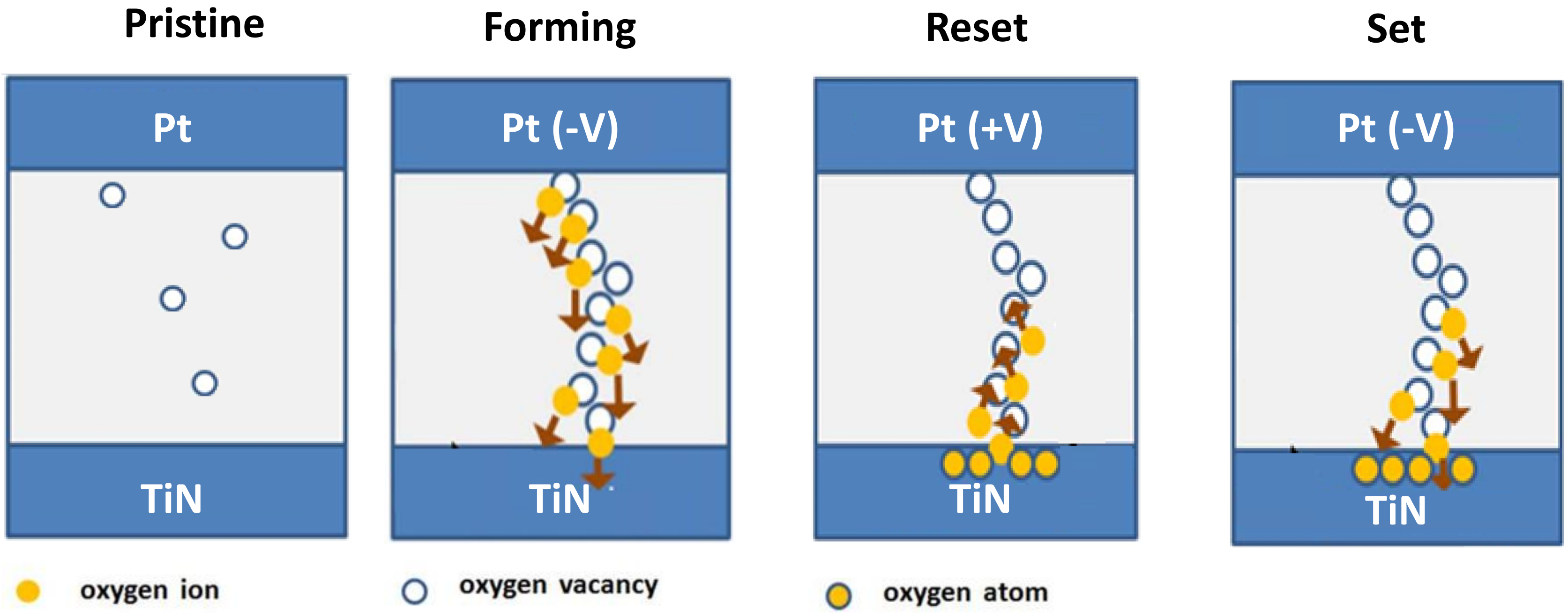



- **Cluster-type Hybrid memristor** (VCM+ECM)




Pt
HfOx
SiO2
TiN
618 nm
TiN


Current [A]
Voltage [V]
ICC : 50 mA
Vset : -0.60 V
Vreset : 1.40 V
Ion/Ioff ratio @ -0.1 V : ~6.46
Vforming : -4.38 V
Cell size: 618 nm
0 ~ -5 V (1)
0 ~ 1.4 V (2)
1.4 ~ 0 V (3)
0 ~ -1 V (4)
-1 ~ 0 V (5)


Pristine
Forming
Reset
Set
Pt
Pt (-V)
Pt (+V)
Pt (-V)
TiN
TiN
TiN
TiN
oxygen ion
oxygen vacancy
oxygen atom

# 1.2 Electrochemical Metallization Memory Cell